


HuaQin Confidential

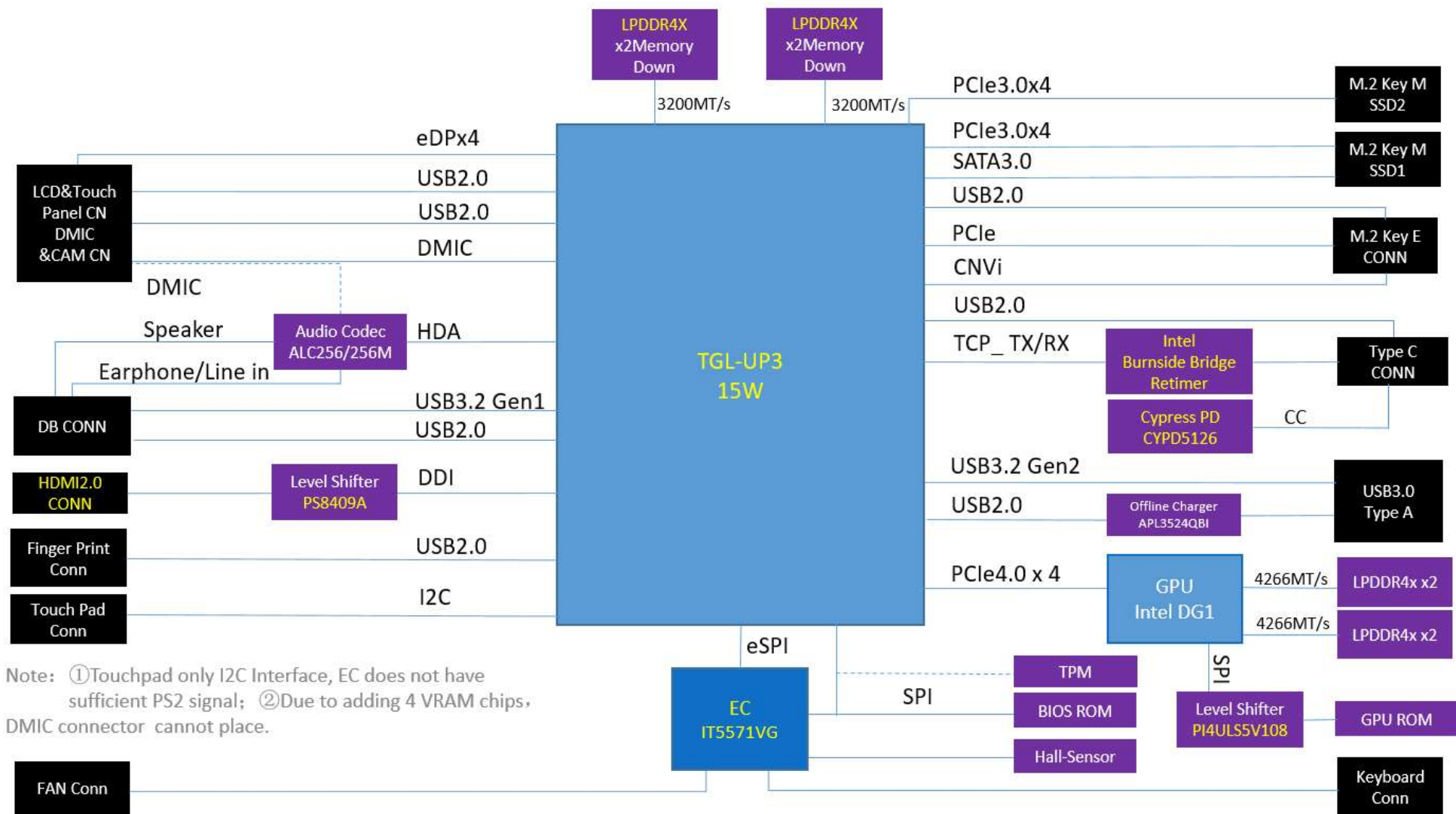
M/B Schematics Document

Intel TGL U-Processor with LPDDR4x

REV 4.0

2020-0825

 HUAQIN 华勤通信		Huaqin Telecom Technology Com.,Ltd.	
Page name:		Cover page	
Size: A4	Project Name:	Swift 3X_TGL-UP3	REV: V4.0
Date:	Friday, August 28, 2020		Sheet: 1 of 84



Note: ①Touchpad only I2C Interface, EC does not have sufficient PS2 signal; ②Due to adding 4 VRAM chips, DMIC connector cannot place.

MEM ID

HW_ID3	HW_ID2	HW_ID1	HW_ID0	Description	Total
0	0	0	0	SAMSUNG LPDDR4 3733 1GB K4F8E304HB-MGCJ LF+HF D20	4GB
0	0	0	1	HYNIX LPDDR4 3733 1GB H9HCNNN8KUMLHR-NME LF+HF DDP	4GB
0	0	1	0	MICRON LPDDR4 4266 2GB MT53E512M32D2NP-046 WT:E LF+HF Z11N	8GB
0	1	0	0	HYNIX LPDDR4 3733 2GB H9HCNNNBPUMLHR-NME LF+HF DE	8GB
0	1	0	0		16GB
1	0	0	0	HYNIX LPDDR4X 4266 4GB H9HCNNNCPMALHR-NEE LF+HF QDP	
				4x 16Gb (reserve)	

GPU ID

HW_ID4	Description
0	UMA
1	DGPU

T.ME/SCHEMATICSLAPTOP

KB BL ID

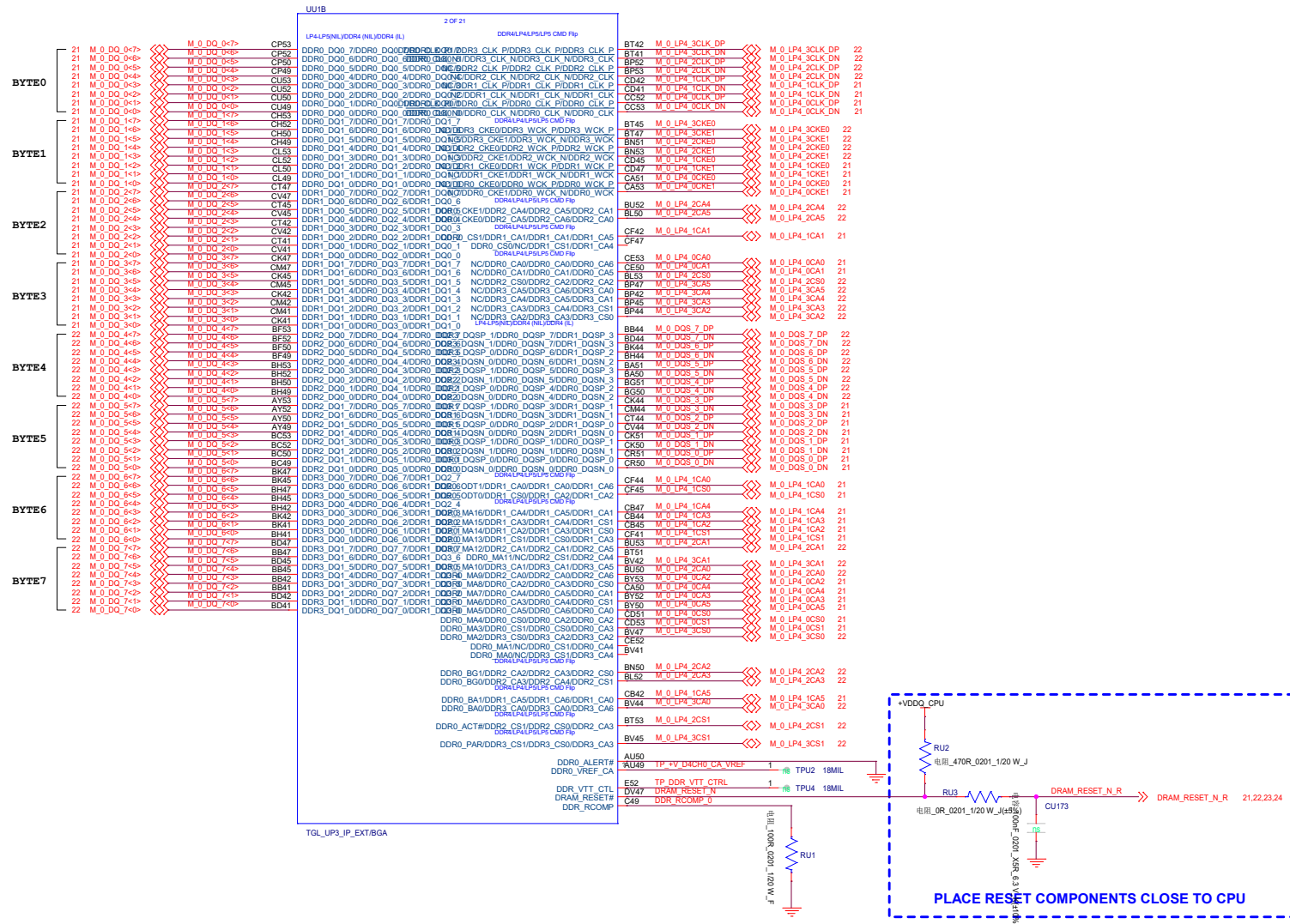
HW_ID6	Description
0	No keyboard Backlight
1	Keyboard Backlight

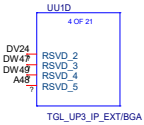
Reserve ID

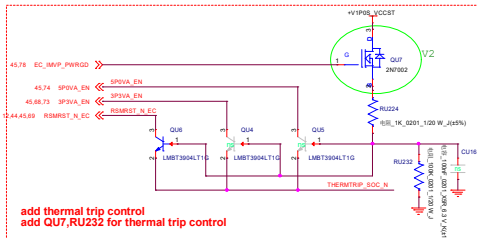
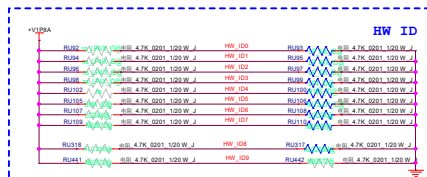
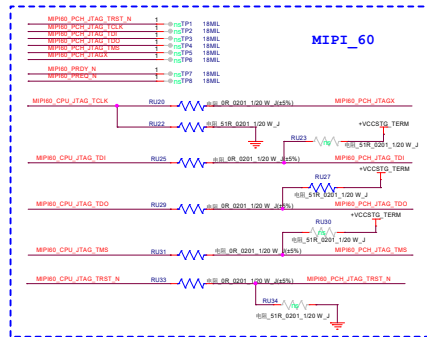
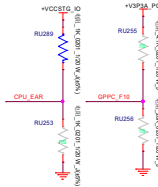
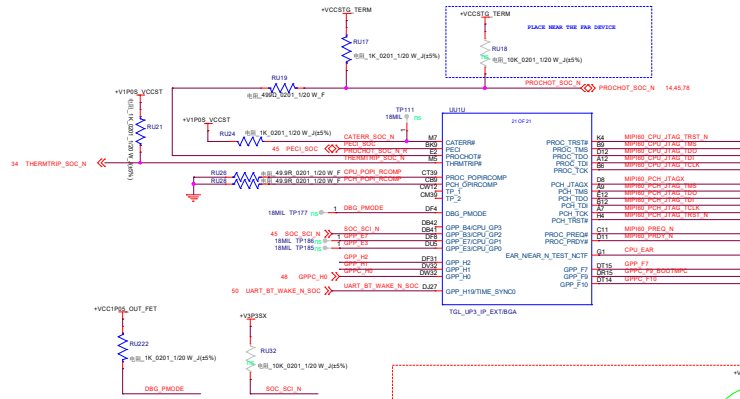
HW_ID7	Description
0	Reserve
1	Reserve

T.ME/SCHEMATICSLAPTOP

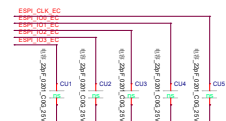
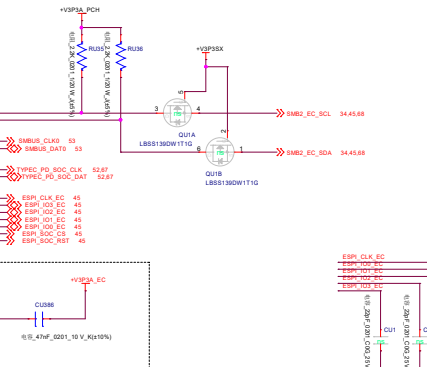
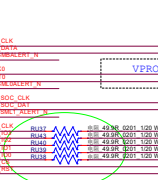
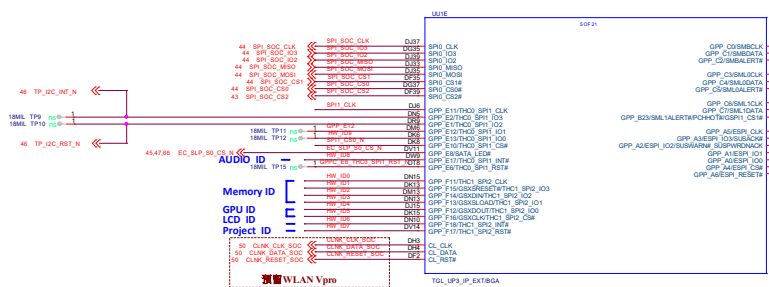
CHA





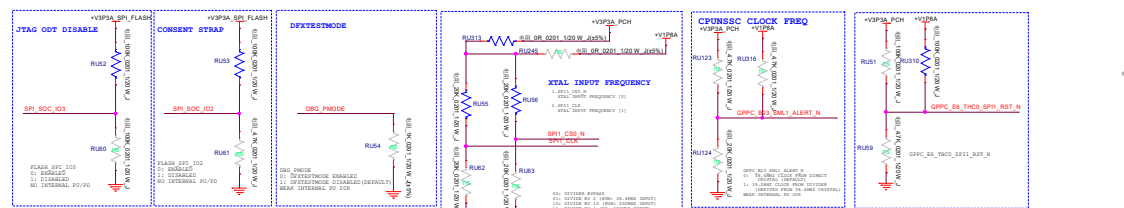
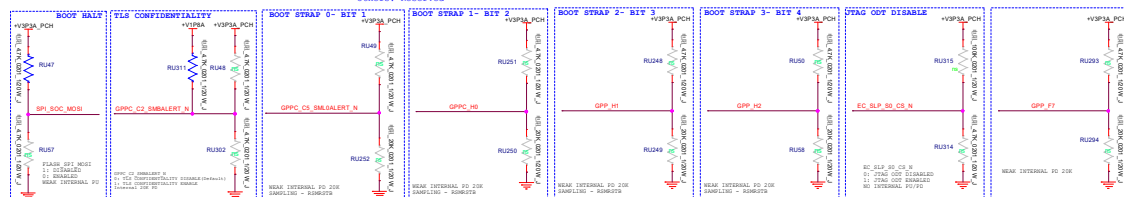


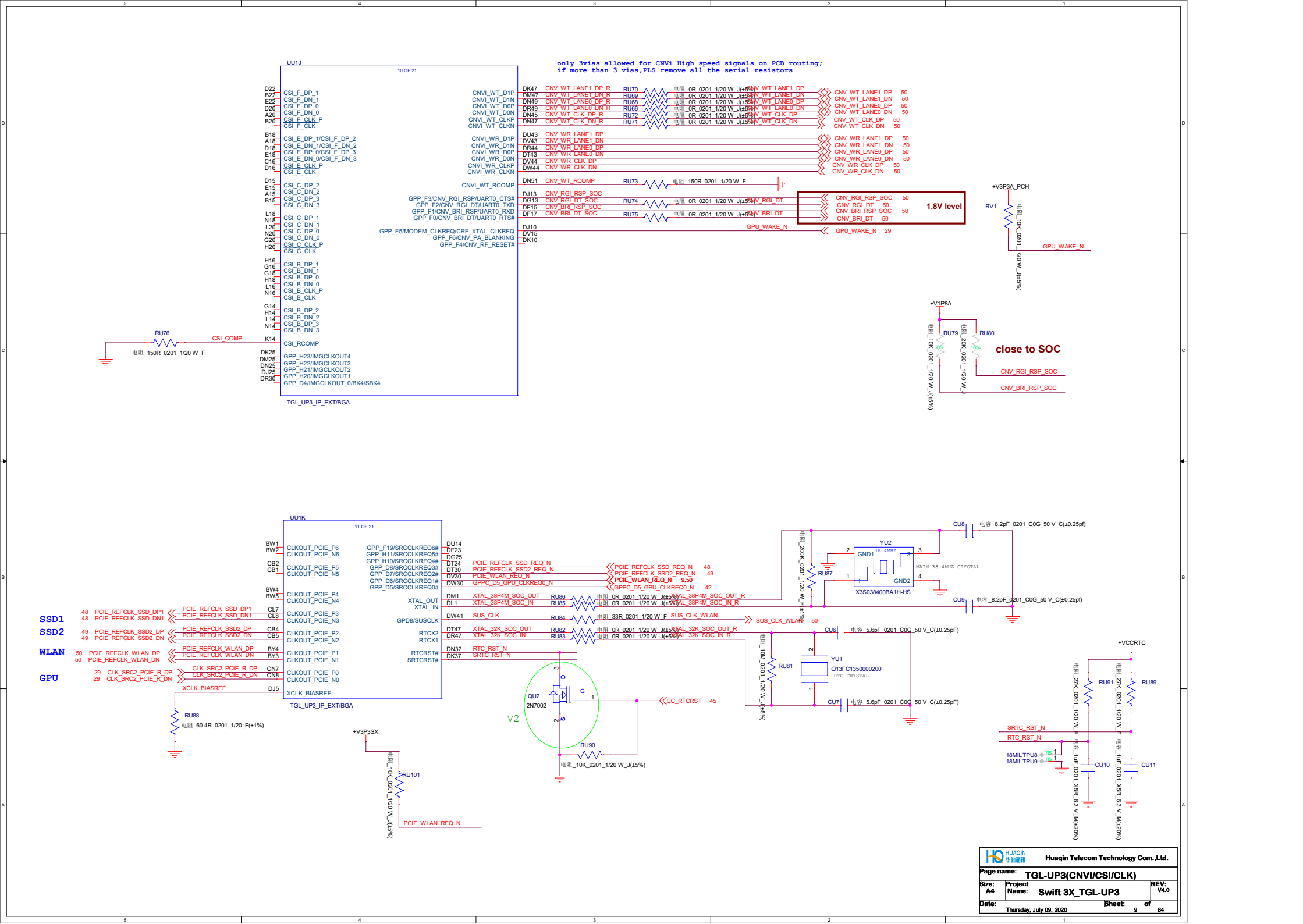
add thermal trip control
add QUT_RU232 for thermal trip control



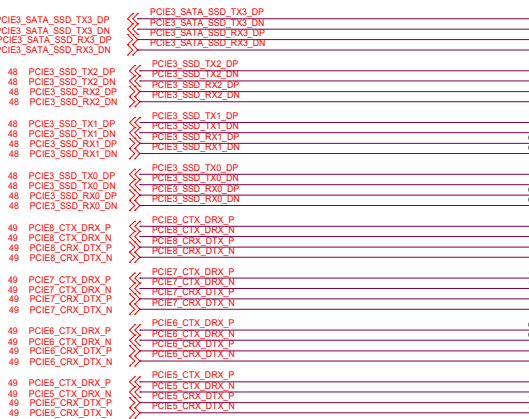
0000 = Master Attached Flash Configuration (BIOS / CSME on SPI).
1000 = Slave Attached Flash Configuration (BIOS / CSME on eSPI attached device).
0100 = BIOS on eSPI Peripheral Channel; CSME on master attached SPI.
1100 = BIOS on eSPI Peripheral Channel; CSME on slave attached SPI.
010001 = Reserved

PCH STRAP





SSD1



teknisi indonesia

WLAN

USB3.1 Type-A for DB

USB3.1 Type-A AOU

GPU



UU1J

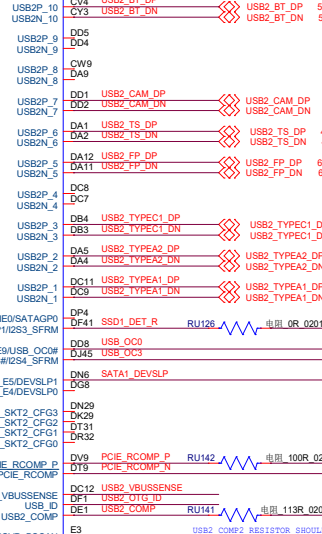
9 OF 21

TGL_UP3_IP_EXT/8GA

UU1H

8 OF 21

TGL_UP3_IP_EXT/8GA



USB2_OTG_ID

USB2_VBUSSENSE

USB2_OTG_ID

USB2_COMP

RSVD_BSCAN

E3

USB2_OTG_ID

USB2_VBUSSENSE

USB2_OTG_ID

USB2_COMP

RSVD_BSCAN

E3

USB2_OTG_ID

USB2_VBUSSENSE

USB2_OTG_ID

USB2_COMP

RSVD_BSCAN

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RSVD_BSCAN

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USB2_VBUSSENSE

USB2_OTG_ID

USB2_COMP

RSVD_BSCAN

E3

USB2_OTG_ID

USB2_VBUSSENSE

USB2_OTG_ID

USB2_COMP

RSVD_BSCAN

E3

USB2_OTG_ID

USB2_VBUSSENSE

USB2_OTG_ID

USB2_COMP

RSVD_BSCAN

E3

USB2_OTG_ID

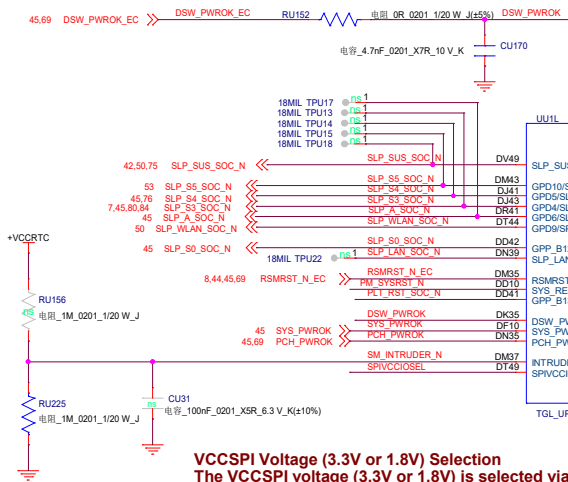
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USB2_OTG_ID

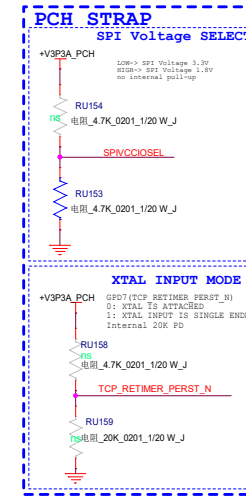
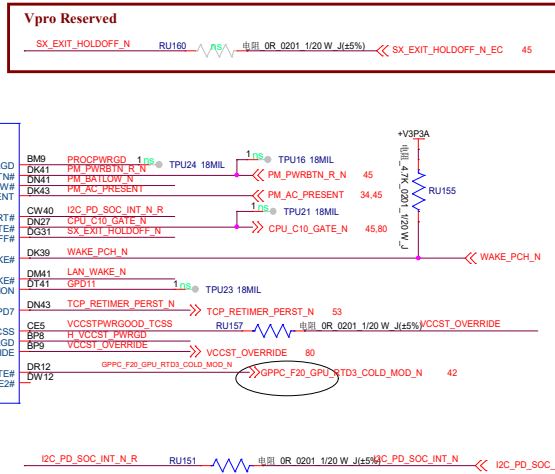
USB2_COMP

RSVD_BSCAN

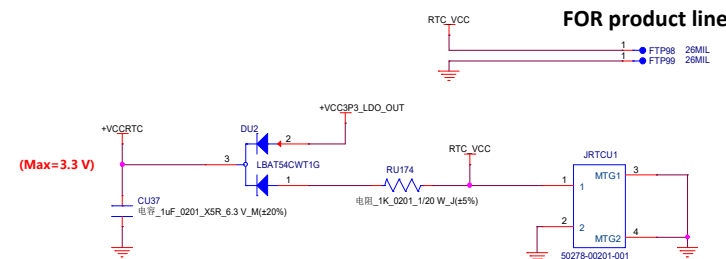
E3

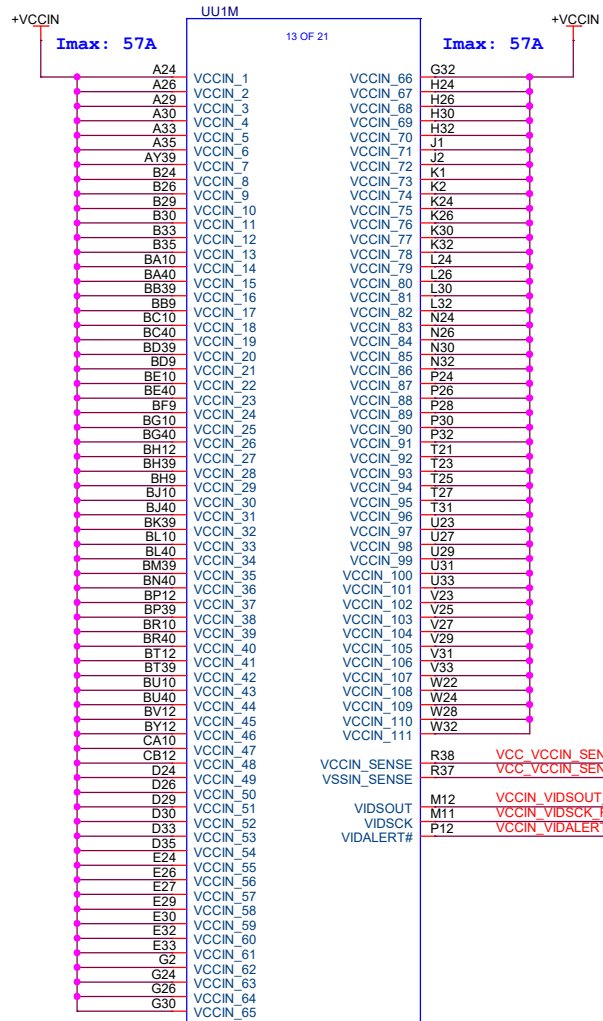


VCCSPI Voltage (3.3V or 1.8V) Selection
 The VCCSPI voltage (3.3V or 1.8V) is selected via a strap on INTRUDER#:
 0 = SPI voltage is 3.3V
 1 = SPI voltage is 1.8V

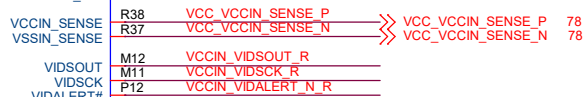


RTC

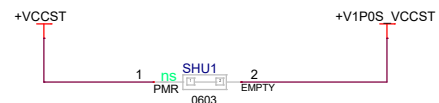
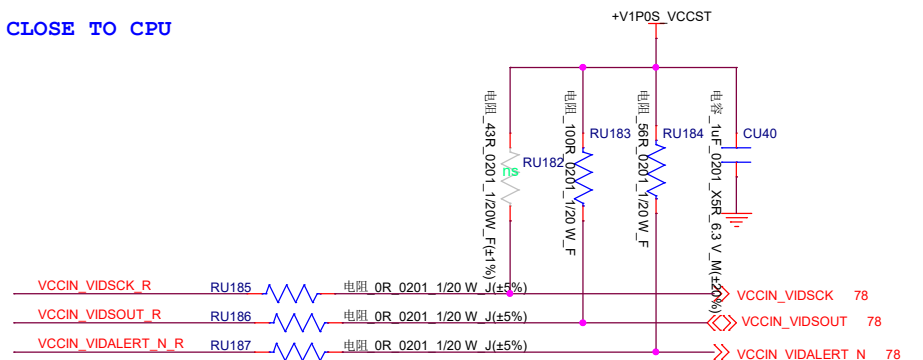


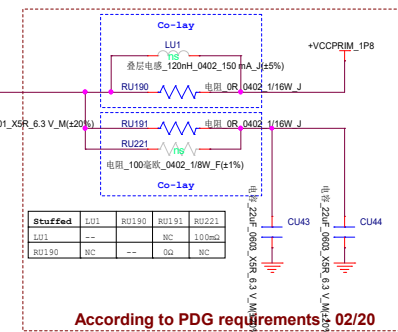
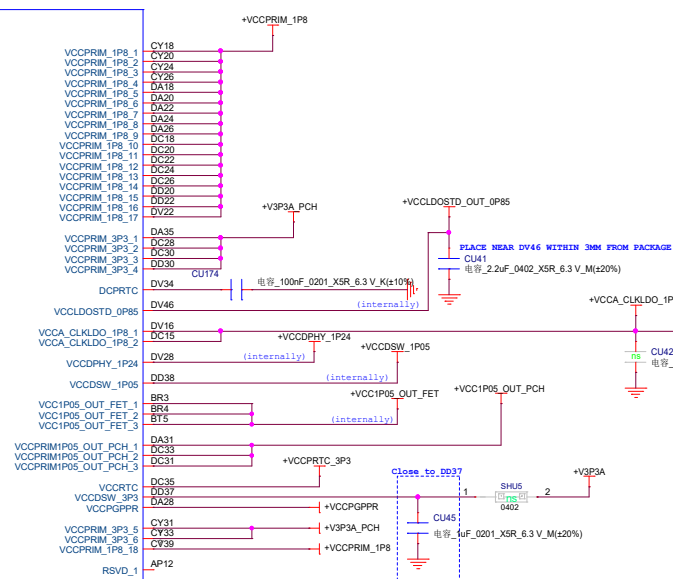
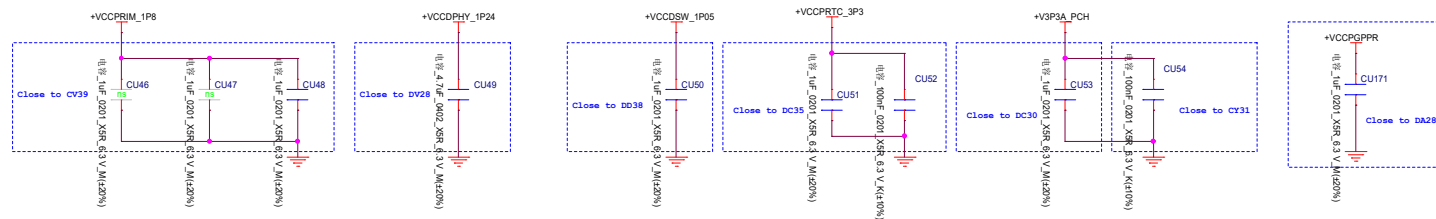
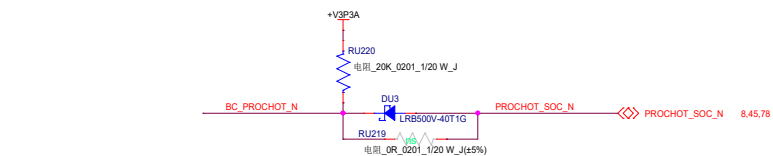
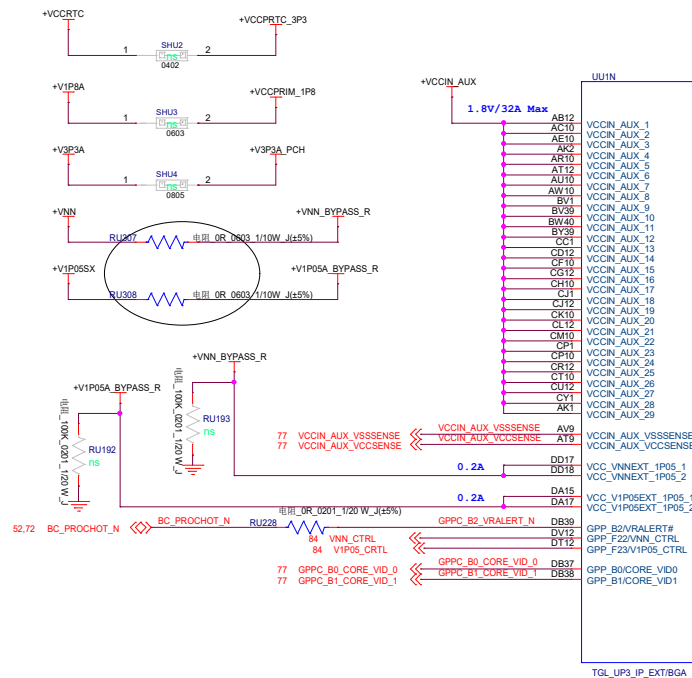


TGL_UP3_IP_EXT/BGA



CLOSE TO CPU

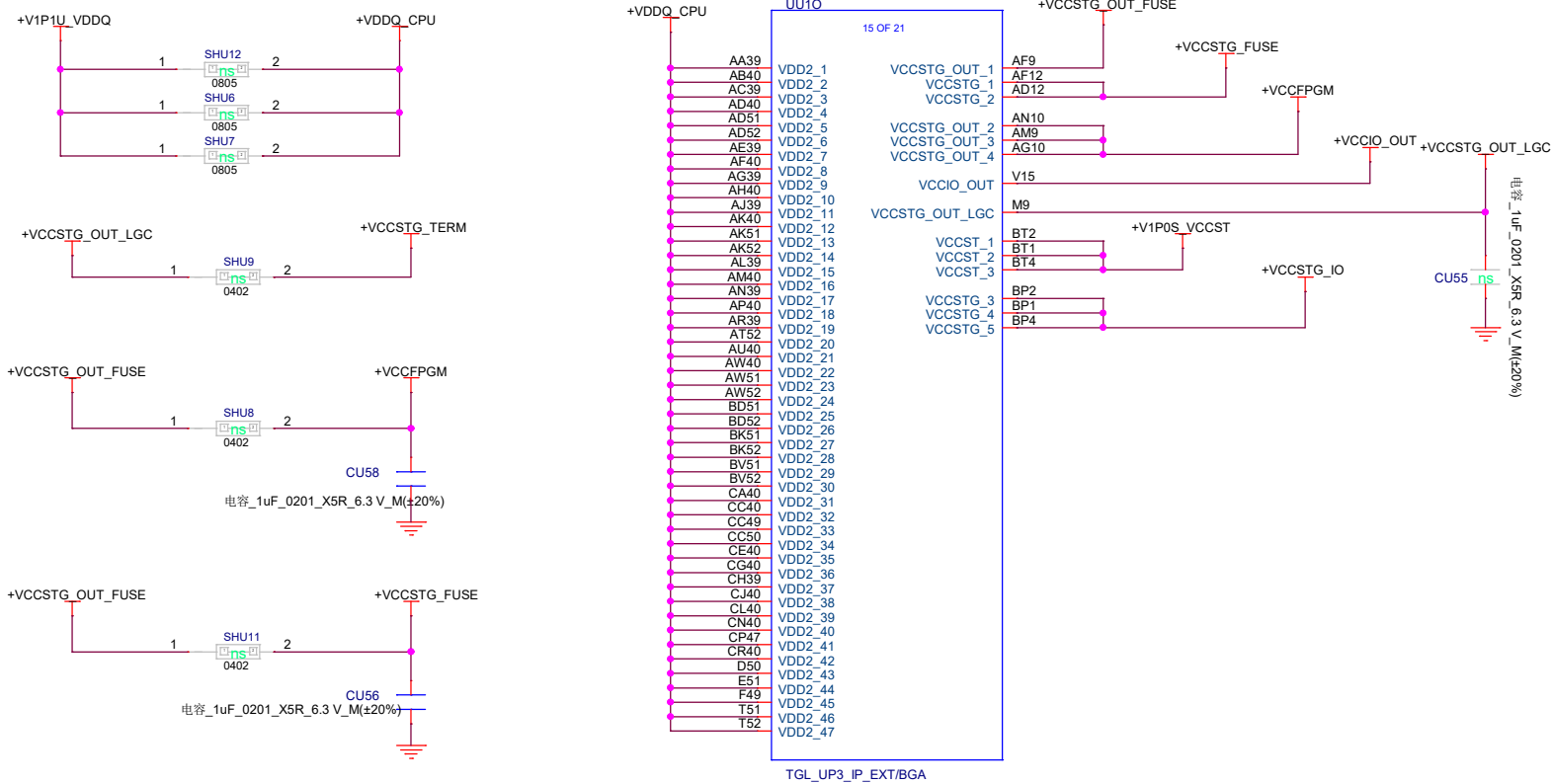


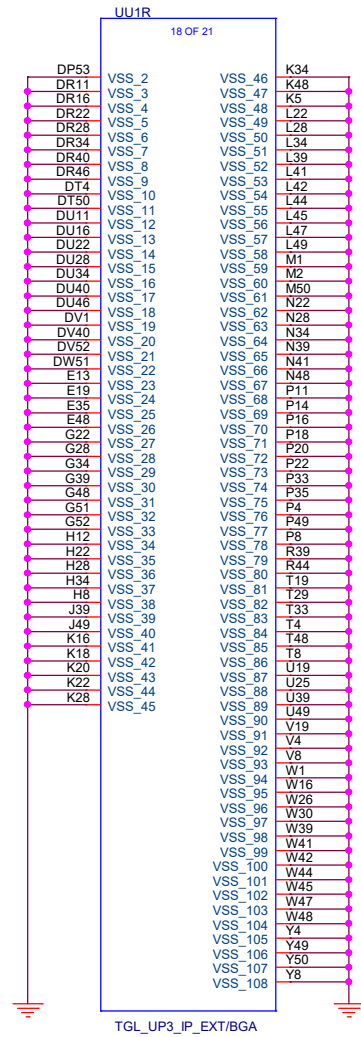
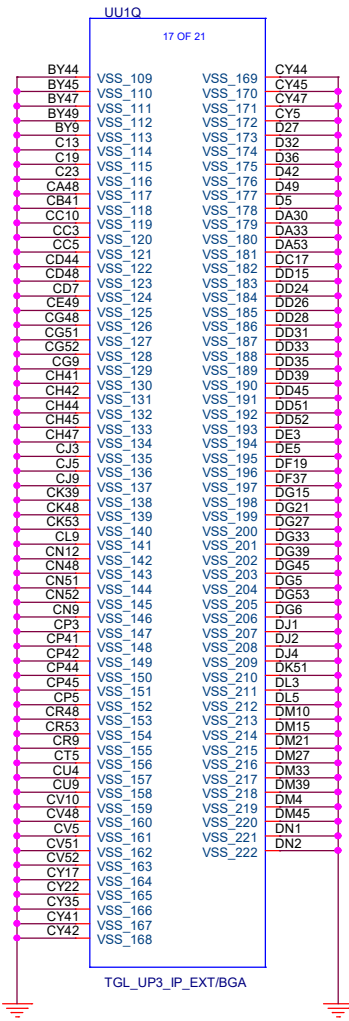
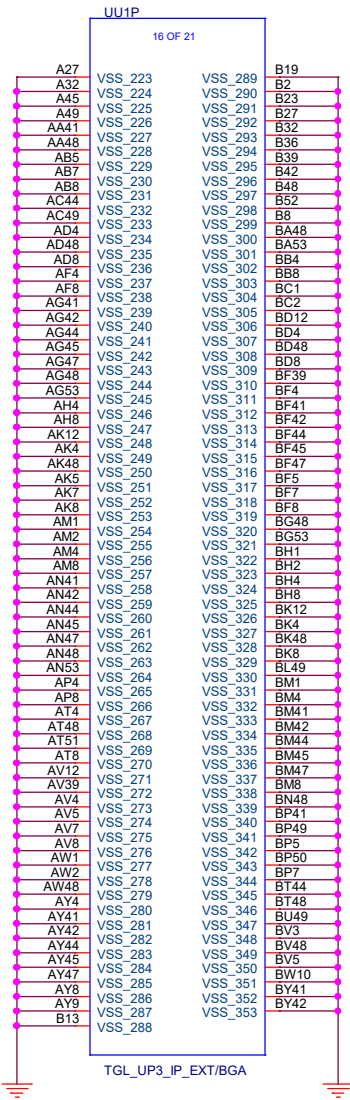


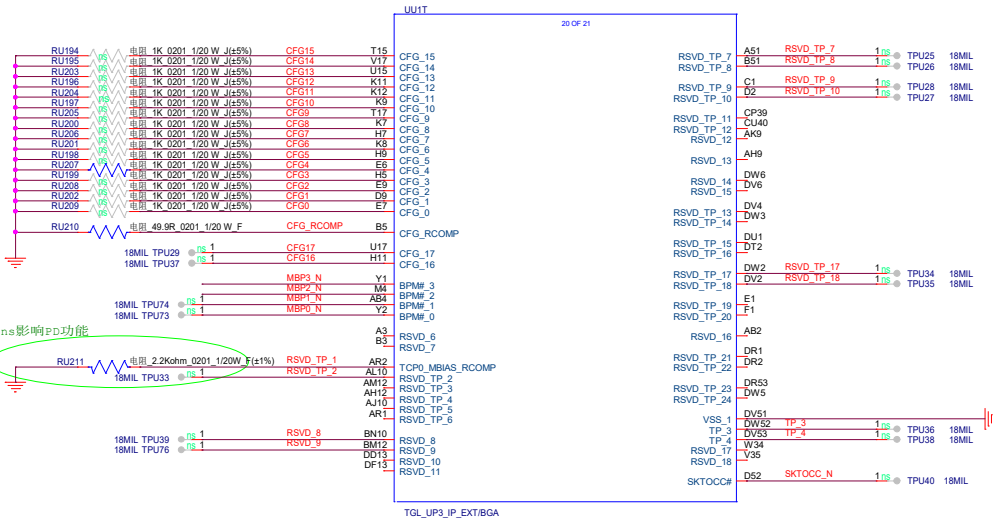
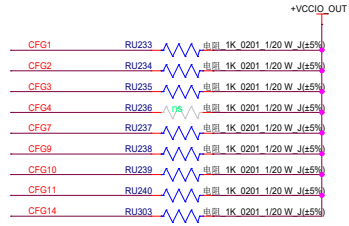
According to PDG requirements 02/20

Audio power for 1.8V and reserve 3.3V

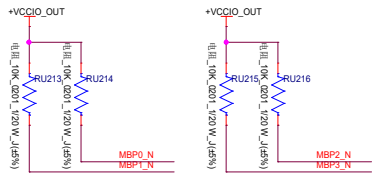
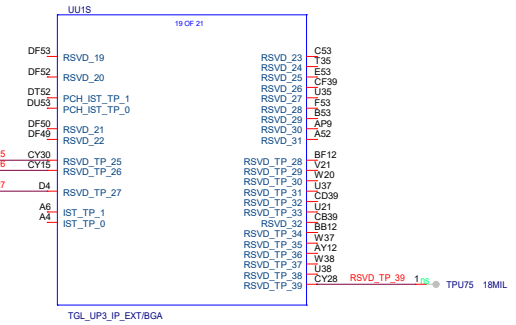


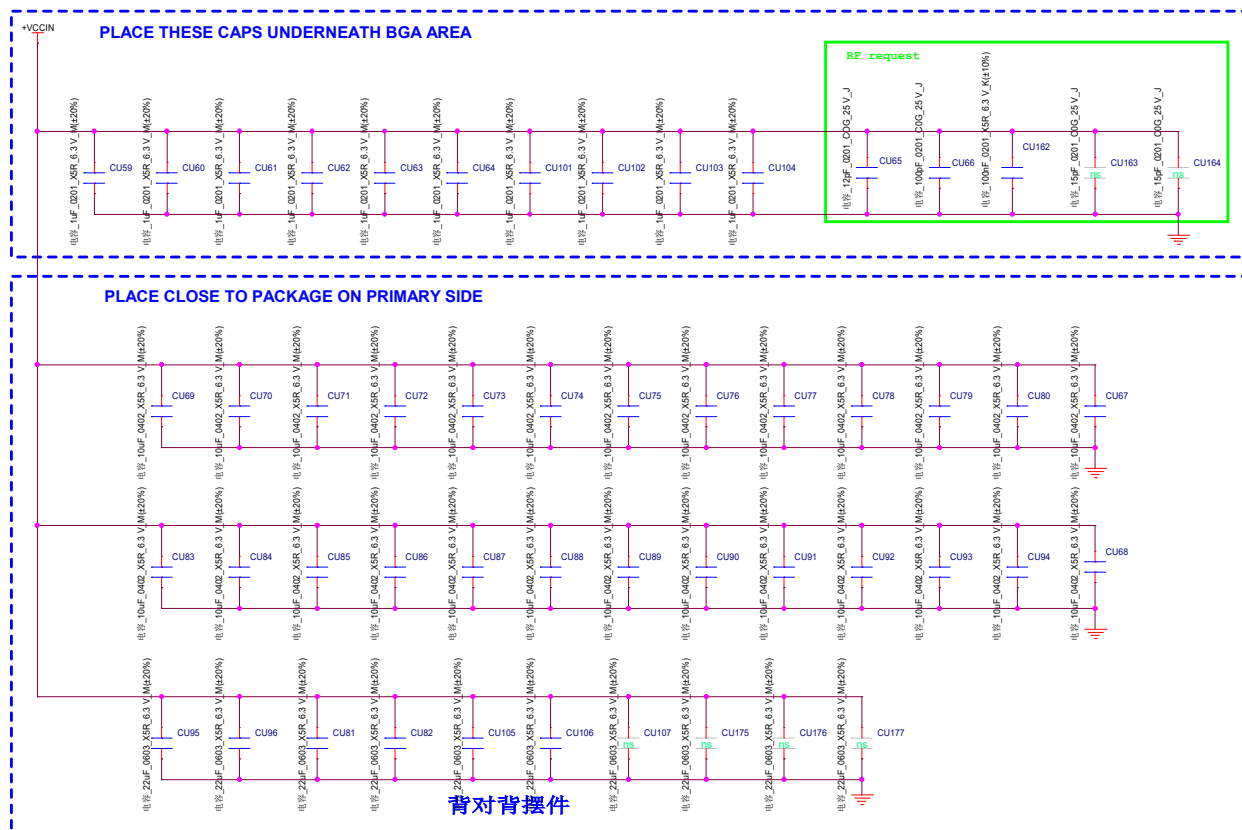




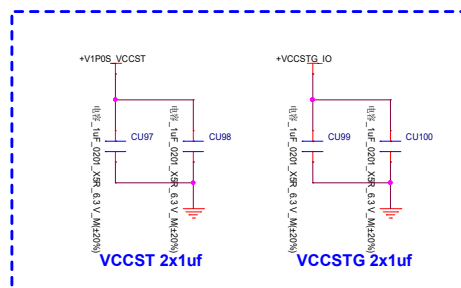


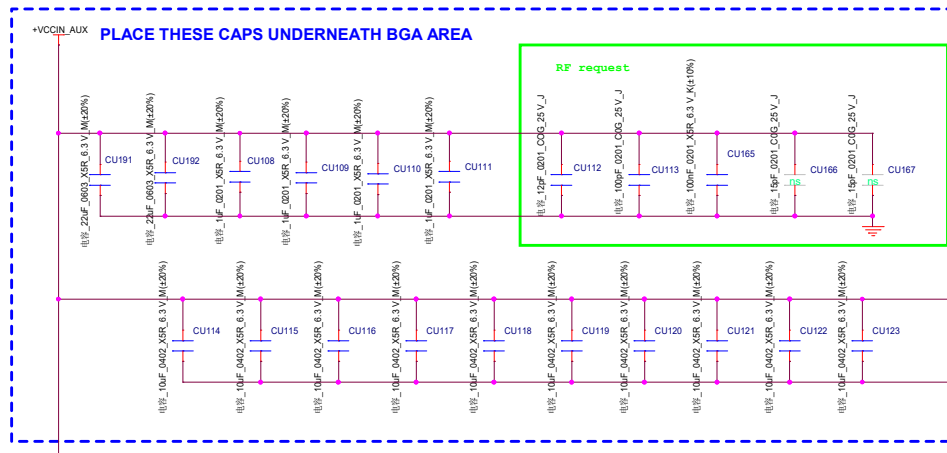
V2----RU211上件, ns影响PD功能



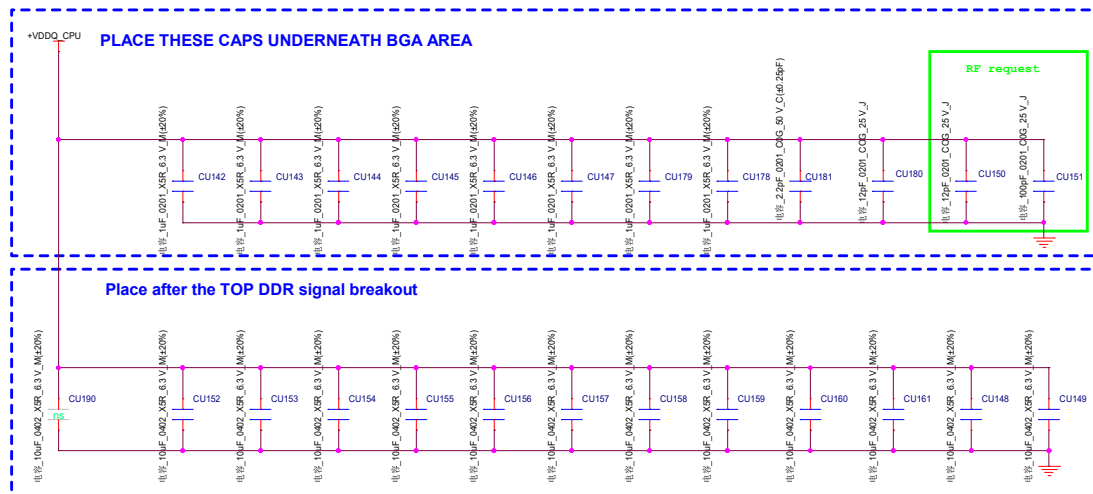
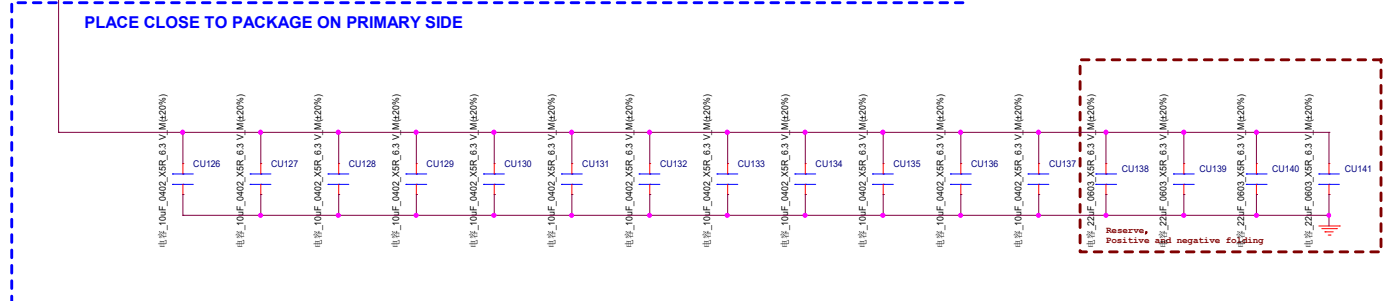


+VCCIN		
	PDG	S5
1uF		10
10uF	12	26
22uF	8	6
47uF		
220uF	2	1

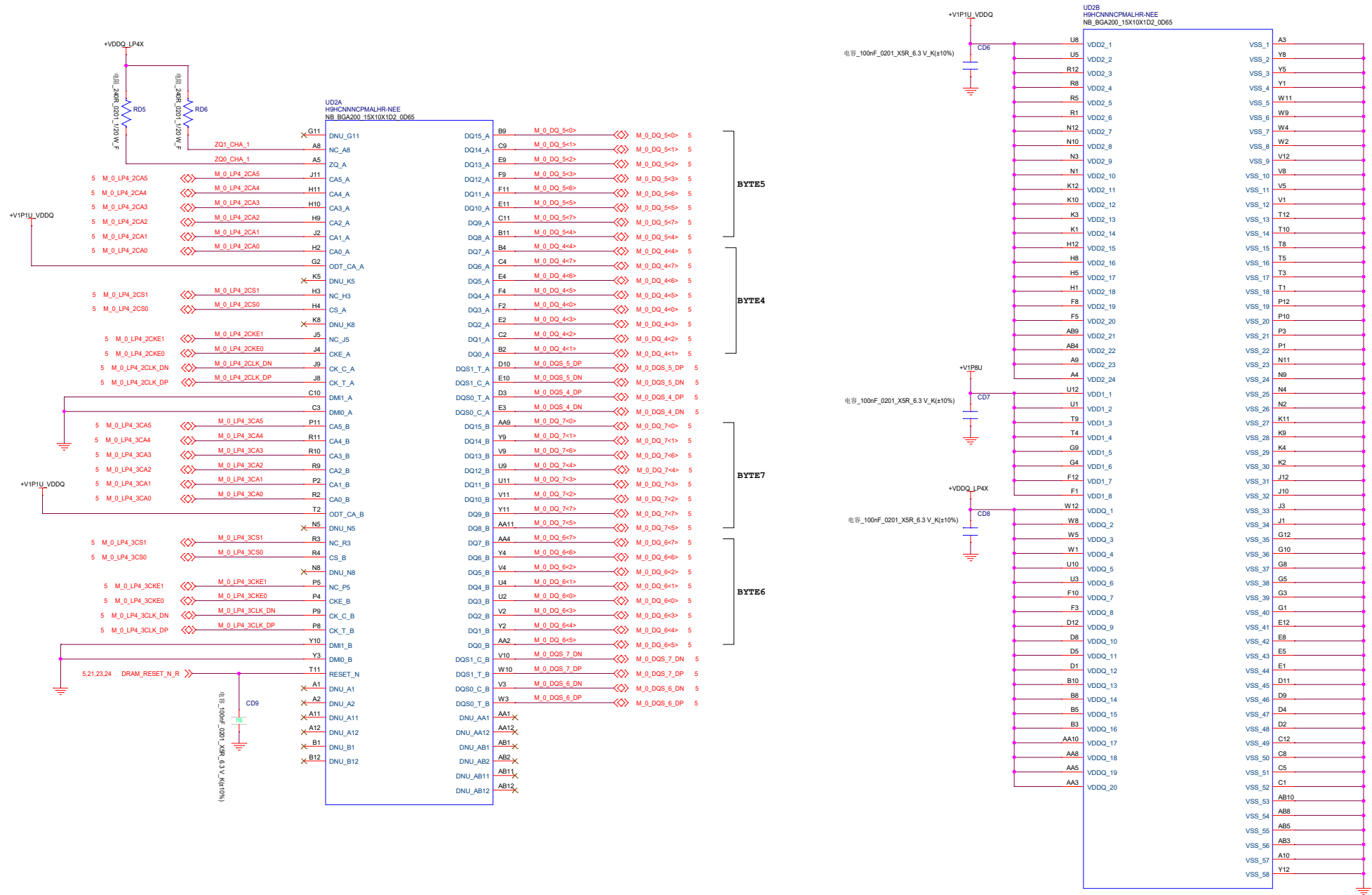


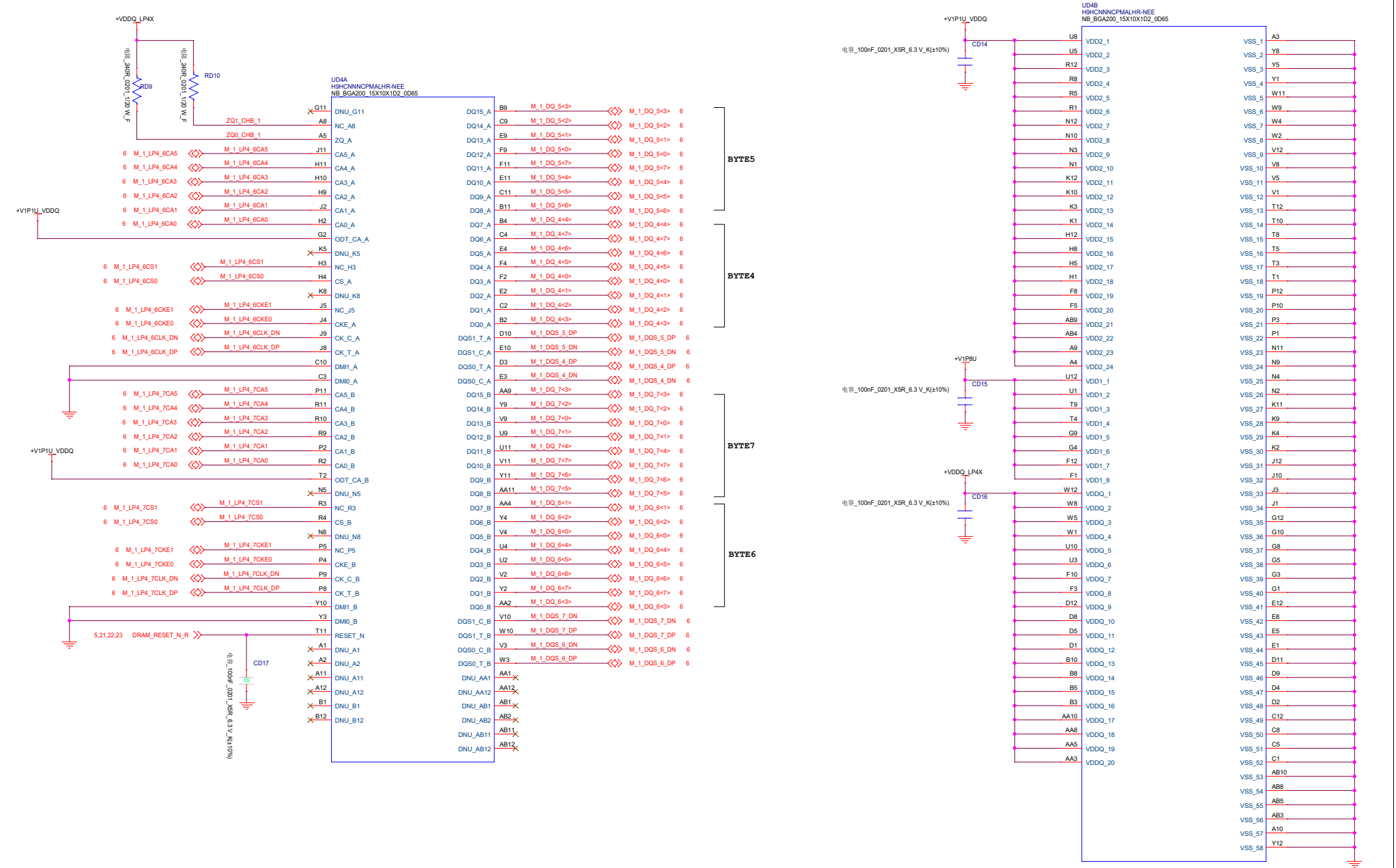


	PDG	S5
1uF		4
10uF	15(T)+10(B)	25
22uF	12	10
47uF	3	
220uF	1	



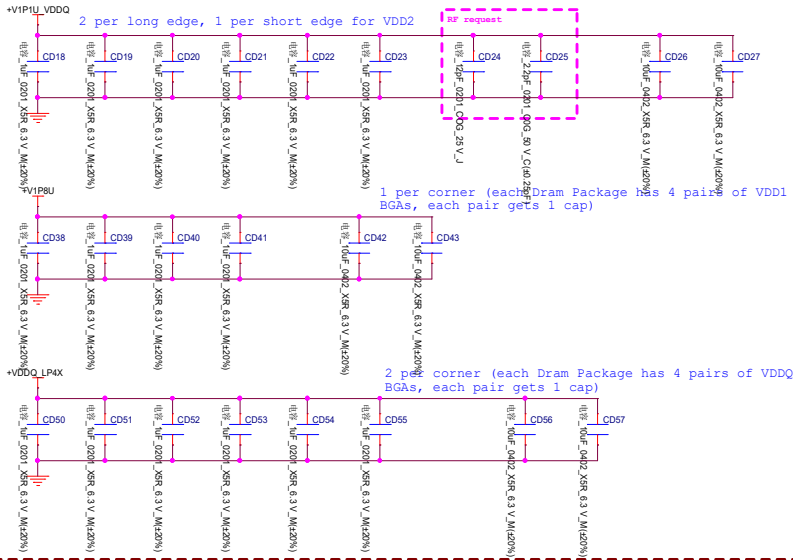
	PDG	S5
1uF	8	8
10uF	13	12
22uF		5(power IC location)
47uF	2	



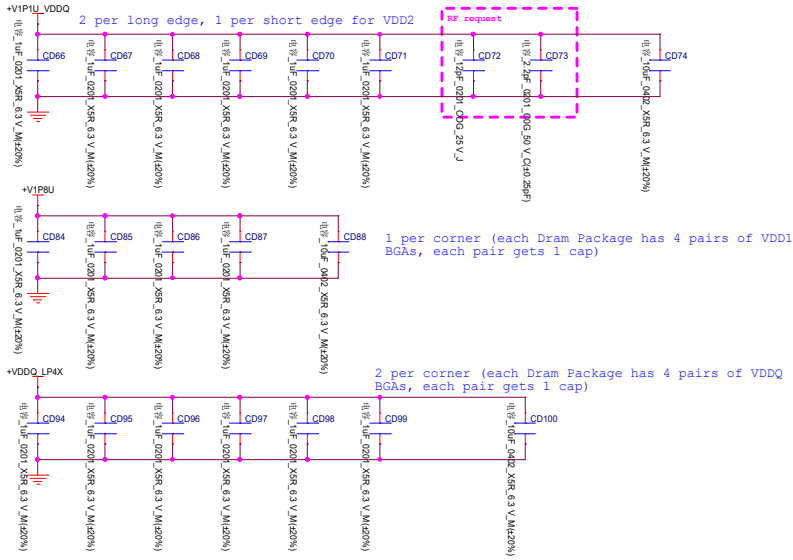


DECOUPLING CAPACITORS FOR LPDDR4x CHANNEL A

Place as close as possible to UD1

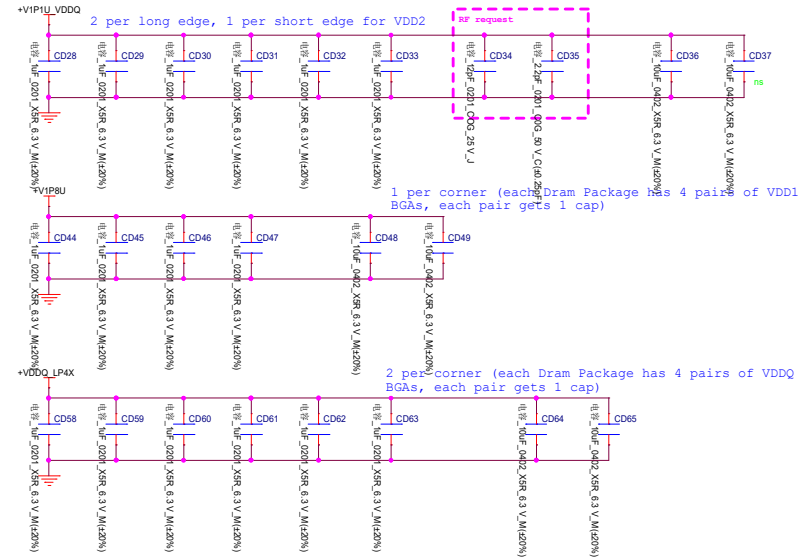


Place as close as possible to UD2



DECOUPLING CAPACITORS FOR LPDDR4x CHANNEL B

Place as close as possible to UD3



Place as close as possible to UD4

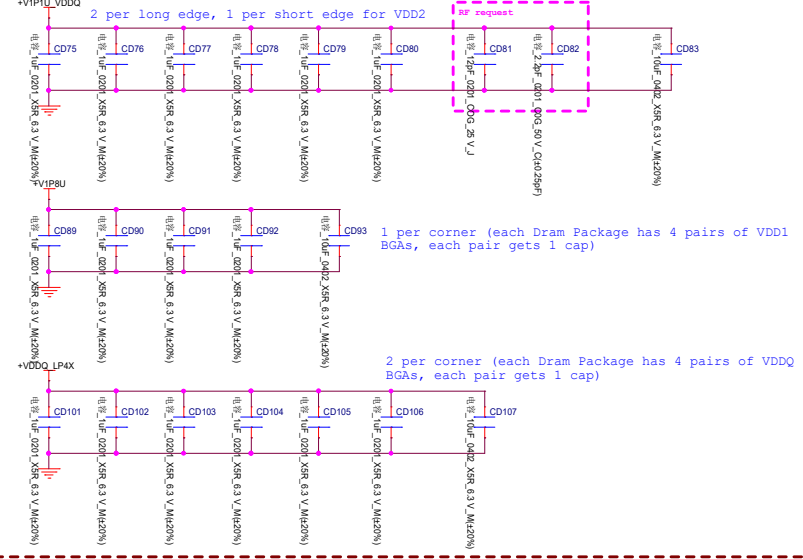
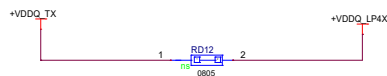



Table 48. LPDDR4X Memory Down Power Plane Decoupling


Memory Configuration	Power Domain	Decoupling Location	Qty x μ F (size)
LPDDR4X x32 Decoupling Config-1	VDD2	6 caps per Dram, 2 per long edge, 1 per short edge evenly distribute among all Drams	24x 1 μ F (0402)
	VDDQ	4 per Dram, 2 per corner (each Dram Package has 4 pairs of VDD1 BGAs, each pair gets 1 cap) evenly distribute among all Drams	5x 10 μ F (0603)
	VDD1	4 per Dram, 1 per corner (each Dram Package has 4 pairs of VDD1 BGAs, each pair gets 1 cap)	16x 1 μ F (0402)
			5x 10 μ F (0603)



5	4	3	2	1
D				
C				
B				
A				
5	4	3	2	1

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Page name: BLANK			
Size: A4	Project Name: Swift 3X_TGL-UP3		REV: V4.0
Date:	Sheet:		of
Thursday, July 09, 2020		26	84

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

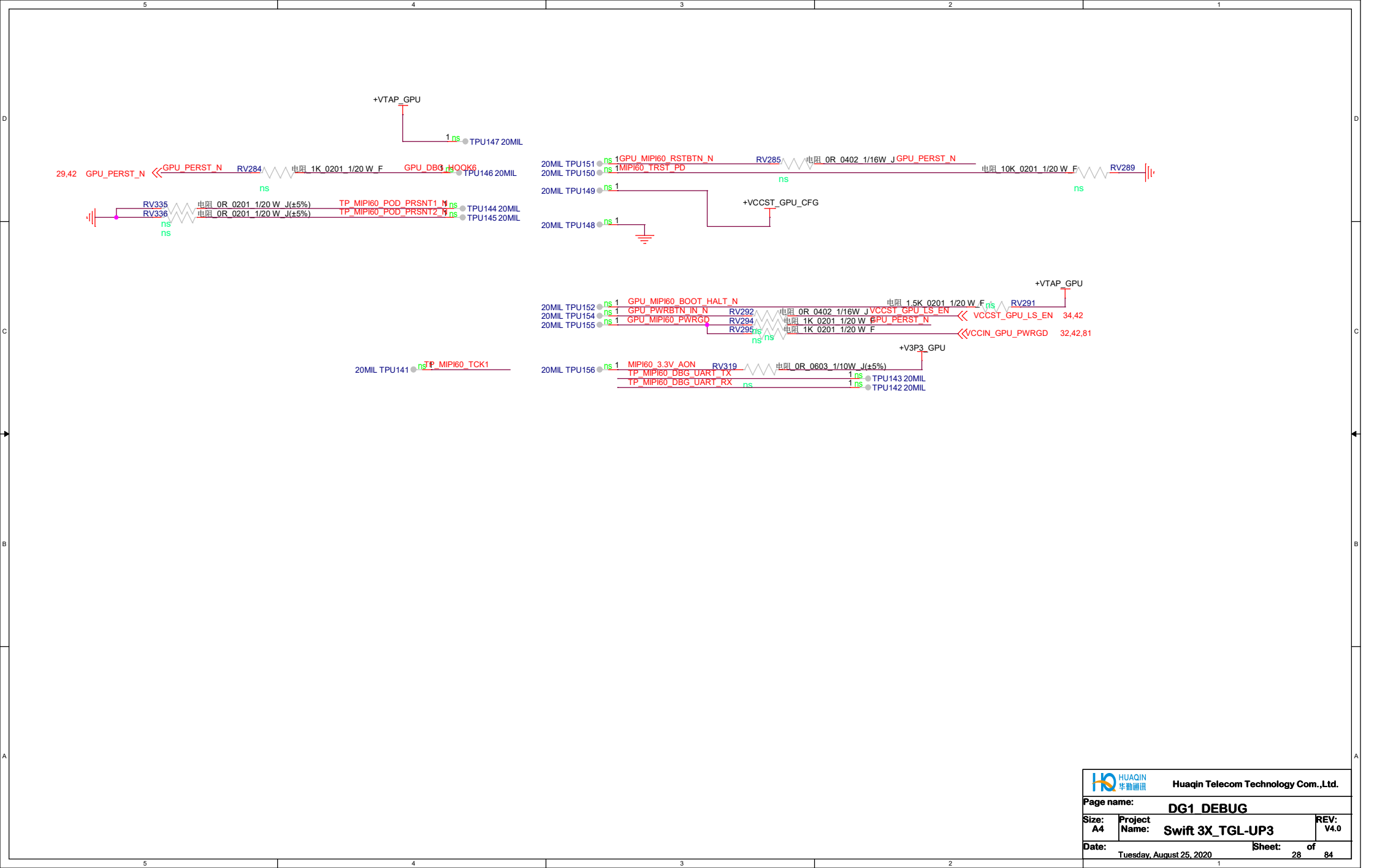


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Date: Thursday, July 09, 2020		Sheet: 27 of 84



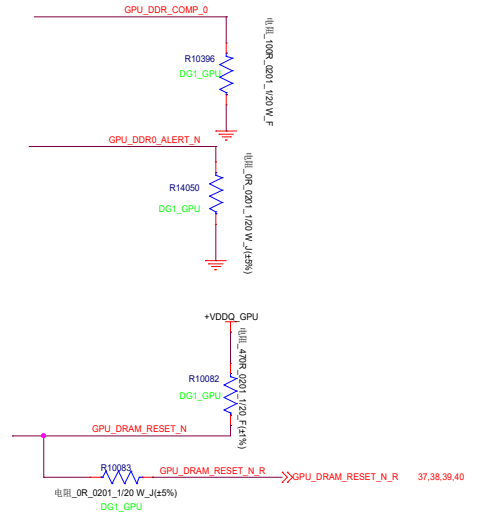
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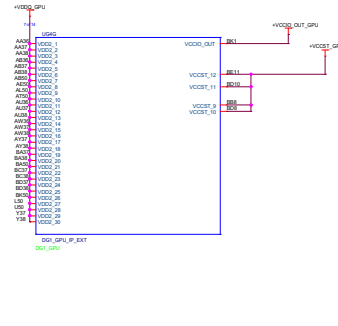
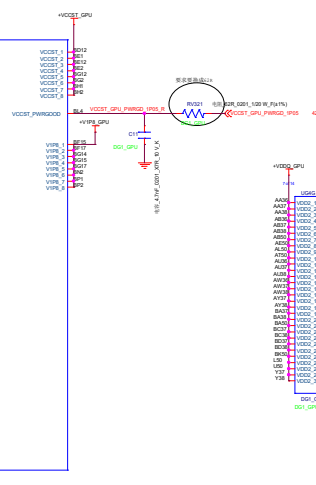
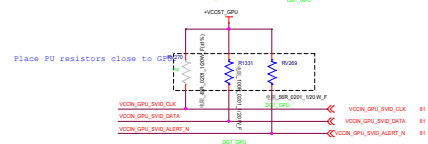
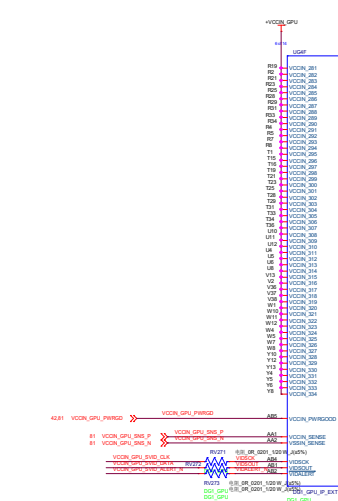
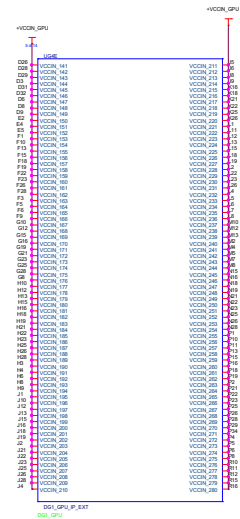
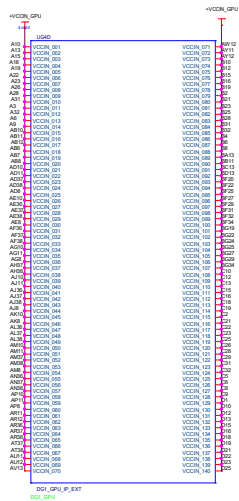
UG4A

37	GPU_M_0_DQ_0<7>	GPU_M_0_DQ_0<7>	C37	DDR0_DQ0_7
37	GPU_M_0_DQ_0<6>	GPU_M_0_DQ_0<6>	D37	DDR0_DQ0_6
37	GPU_M_0_DQ_0<5>	GPU_M_0_DQ_0<5>	A37	DDR0_DQ0_5
37	GPU_M_0_DQ_0<4>	GPU_M_0_DQ_0<4>	B37	DDR0_DQ0_4
37	GPU_M_0_DQ_0<3>	GPU_M_0_DQ_0<3>	B36	DDR0_DQ0_3
37	GPU_M_0_DQ_0<2>	GPU_M_0_DQ_0<2>	D35	DDR0_DQ0_2
37	GPU_M_0_DQ_0<1>	GPU_M_0_DQ_0<1>	C35	DDR0_DQ0_1
37	GPU_M_0_DQ_0<0>	GPU_M_0_DQ_0<0>	C34	DDR0_DQ0_0
37	GPU_M_0_DQ_1<7>	GPU_M_0_DQ_1<7>	D43	DDR0_DQ1_7
37	GPU_M_0_DQ_1<6>	GPU_M_0_DQ_1<6>	A43	DDR0_DQ1_6
37	GPU_M_0_DQ_1<5>	GPU_M_0_DQ_1<5>	B43	DDR0_DQ1_5
37	GPU_M_0_DQ_1<4>	GPU_M_0_DQ_1<4>	B41	DDR0_DQ1_4
37	GPU_M_0_DQ_1<3>	GPU_M_0_DQ_1<3>	A41	DDR0_DQ1_3
37	GPU_M_0_DQ_1<2>	GPU_M_0_DQ_1<2>	C41	DDR0_DQ1_2
37	GPU_M_0_DQ_1<1>	GPU_M_0_DQ_1<1>	H33	DDR0_DQ1_1
37	GPU_M_0_DQ_1<0>	GPU_M_0_DQ_1<0>	H33	DDR0_DQ1_0
37	GPU_M_1_DQ_0<7>	GPU_M_1_DQ_0<7>	L33	DDR1_DQ0_7
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37	GPU_M_1_DQ_0<5>	GPU_M_1_DQ_0<5>	K31	DDR1_DQ0_5
37	GPU_M_1_DQ_0<4>	GPU_M_1_DQ_0<4>	H31	DDR1_DQ0_4
37	GPU_M_1_DQ_0<3>	GPU_M_1_DQ_0<3>	H31	DDR1_DQ0_3
37	GPU_M_1_DQ_0<2>	GPU_M_1_DQ_0<2>	H38	DDR1_DQ0_2
37	GPU_M_1_DQ_0<1>	GPU_M_1_DQ_0<1>	G38	DDR1_DQ0_1
37	GPU_M_1_DQ_0<0>	GPU_M_1_DQ_0<0>	L38	DDR1_DQ0_0
37	GPU_M_1_DQ_1<7>	GPU_M_1_DQ_1<7>	K38	DDR1_DQ1_7
37	GPU_M_1_DQ_1<6>	GPU_M_1_DQ_1<6>	L38	DDR1_DQ1_6
37	GPU_M_1_DQ_1<5>	GPU_M_1_DQ_1<5>	K38	DDR1_DQ1_5
37	GPU_M_1_DQ_1<4>	GPU_M_1_DQ_1<4>	L38	DDR1_DQ1_4
37	GPU_M_1_DQ_1<3>	GPU_M_1_DQ_1<3>	K36	DDR1_DQ1_3
37	GPU_M_1_DQ_1<2>	GPU_M_1_DQ_1<2>	H36	DDR1_DQ1_2
37	GPU_M_1_DQ_1<1>	GPU_M_1_DQ_1<1>	G36	DDR1_DQ1_1
37	GPU_M_1_DQ_1<0>	GPU_M_1_DQ_1<0>	G36	DDR1_DQ1_0
37	GPU_M_2_DQ_0<7>	GPU_M_2_DQ_0<7>	AF47	DDR2_DQ0_7
37	GPU_M_2_DQ_0<6>	GPU_M_2_DQ_0<6>	AF46	DDR2_DQ0_6
37	GPU_M_2_DQ_0<5>	GPU_M_2_DQ_0<5>	AF50	DDR2_DQ0_5
37	GPU_M_2_DQ_0<4>	GPU_M_2_DQ_0<4>	AD49	DDR2_DQ0_4
37	GPU_M_2_DQ_0<3>	GPU_M_2_DQ_0<3>	AD49	DDR2_DQ0_3
37	GPU_M_2_DQ_0<2>	GPU_M_2_DQ_0<2>	AD46	DDR2_DQ0_2
37	GPU_M_2_DQ_0<1>	GPU_M_2_DQ_0<1>	AD50	DDR2_DQ0_1
37	GPU_M_2_DQ_0<0>	GPU_M_2_DQ_0<0>	AD47	DDR2_DQ0_0
37	GPU_M_2_DQ_1<7>	GPU_M_2_DQ_1<7>	AM47	DDR2_DQ1_7
37	GPU_M_2_DQ_1<6>	GPU_M_2_DQ_1<6>	AM46	DDR2_DQ1_6
37	GPU_M_2_DQ_1<5>	GPU_M_2_DQ_1<5>	AM50	DDR2_DQ1_5
37	GPU_M_2_DQ_1<4>	GPU_M_2_DQ_1<4>	AM49	DDR2_DQ1_4
37	GPU_M_2_DQ_1<3>	GPU_M_2_DQ_1<3>	AM50	DDR2_DQ1_3
37	GPU_M_2_DQ_1<2>	GPU_M_2_DQ_1<2>	AJ50	DDR2_DQ1_2
37	GPU_M_2_DQ_1<1>	GPU_M_2_DQ_1<1>	AJ46	DDR2_DQ1_1
37	GPU_M_2_DQ_1<0>	GPU_M_2_DQ_1<0>	AJ47	DDR2_DQ1_0
37	GPU_M_3_DQ_0<7>	GPU_M_3_DQ_0<7>	AA43	DDR3_DQ0_7
37	GPU_M_3_DQ_0<6>	GPU_M_3_DQ_0<6>	AA44	DDR3_DQ0_6
37	GPU_M_3_DQ_0<5>	GPU_M_3_DQ_0<5>	V43	DDR3_DQ0_5
37	GPU_M_3_DQ_0<4>	GPU_M_3_DQ_0<4>	V44	DDR3_DQ0_4
37	GPU_M_3_DQ_0<3>	GPU_M_3_DQ_0<3>	V42	DDR3_DQ0_3
37	GPU_M_3_DQ_0<2>	GPU_M_3_DQ_0<2>	AA40	DDR3_DQ0_2
37	GPU_M_3_DQ_0<1>	GPU_M_3_DQ_0<1>	V40	DDR3_DQ0_1
37	GPU_M_3_DQ_0<0>	GPU_M_3_DQ_0<0>	AF43	DDR3_DQ0_0
37	GPU_M_3_DQ_1<7>	GPU_M_3_DQ_1<7>	AF44	DDR3_DQ1_7
37	GPU_M_3_DQ_1<6>	GPU_M_3_DQ_1<6>	AF40	DDR3_DQ1_6
37	GPU_M_3_DQ_1<5>	GPU_M_3_DQ_1<5>	AD43	DDR3_DQ1_5
37	GPU_M_3_DQ_1<4>	GPU_M_3_DQ_1<4>	AD44	DDR3_DQ1_4
37	GPU_M_3_DQ_1<3>	GPU_M_3_DQ_1<3>	AD40	DDR3_DQ1_3
37	GPU_M_3_DQ_1<2>	GPU_M_3_DQ_1<2>	AD40	DDR3_DQ1_2
37	GPU_M_3_DQ_1<1>	GPU_M_3_DQ_1<1>	AD42	DDR3_DQ1_1
37	GPU_M_3_DQ_1<0>	GPU_M_3_DQ_1<0>	AD42	DDR3_DQ1_0

DG1_GPU_IP_EXT
DG1_GPU

DDR3_CLK_P	T44	GPU_M_3_LP4X_CLK_DP	GPU_M_3_LP4X_CLK_DP	38
DDR3_CLK_N	T43	GPU_M_3_LP4X_CLK_DN	GPU_M_3_LP4X_CLK_DN	38
DDR2_CLK_P	V47	GPU_M_2_LP4X_CLK_DP	GPU_M_2_LP4X_CLK_DP	38
DDR2_CLK_N	V46	GPU_M_2_LP4X_CLK_DN	GPU_M_2_LP4X_CLK_DN	38
DDR1_CLK_P	J40	GPU_M_1_LP4X_CLK_DP	GPU_M_1_LP4X_CLK_DP	37
DDR1_CLK_N	J42	GPU_M_1_LP4X_CLK_DN	GPU_M_1_LP4X_CLK_DN	37
DDR0_CLK_P	G47	GPU_M_0_LP4X_CLK_DP	GPU_M_0_LP4X_CLK_DP	37
DDR0_CLK_N	G46	GPU_M_0_LP4X_CLK_DN	GPU_M_0_LP4X_CLK_DN	37
DDR3_CKE0	N47	GPU_M_3_LP4X_CKE_0	GPU_M_3_LP4X_CKE_0	38
DDR3_CKE1	N46	GPU_M_2_LP4X_CKE_0	GPU_M_2_LP4X_CKE_0	38
DDR2_CKE0	V46	GPU_M_1_LP4X_CKE_0	GPU_M_1_LP4X_CKE_0	37
DDR2_CKE1	K40	GPU_M_0_LP4X_CKE_0	GPU_M_0_LP4X_CKE_0	37
DDR1_CKE0	N47	GPU_M_3_LP4X_CKE_0	GPU_M_3_LP4X_CKE_0	37
DDR1_CKE1	N46	GPU_M_2_LP4X_CKE_0	GPU_M_2_LP4X_CKE_0	37
DDR0_CKE0	V49	GPU_M_2_LP4X_CA_4	GPU_M_2_LP4X_CA_4	38
DDR0_CKE1	A40	GPU_M_2_LP4X_CA_5	GPU_M_2_LP4X_CA_5	38
DDR2_CA4	G43	GPU_M_1_LP4X_CA_1	GPU_M_1_LP4X_CA_1	37
DDR2_CA5	K43	GPU_M_0_LP4X_CA_0	GPU_M_0_LP4X_CA_0	37
DDR1_CA1	E45	GPU_M_0_LP4X_CA_0	GPU_M_0_LP4X_CA_0	37
NC_5	D48	GPU_M_0_LP4X_CA_1	GPU_M_0_LP4X_CA_1	37
DDR0_CA0	P50	GPU_M_2_LP4X_CS_0	GPU_M_2_LP4X_CS_0	38
DDR0_CA1	N50	GPU_M_3_LP4X_CA_5	GPU_M_3_LP4X_CA_5	38
DDR2_CS0	E50	GPU_M_3_LP4X_CA_4	GPU_M_3_LP4X_CA_4	38
DDR3_CA5	T50	GPU_M_3_LP4X_CA_3	GPU_M_3_LP4X_CA_3	38
DDR3_CA4	N49	GPU_M_3_LP4X_CA_2	GPU_M_3_LP4X_CA_2	38
DDR3_CA2	AE40	GPU_M_3_DQS_1_DP	GPU_M_3_DQS_1_DP	38
DDR3_DQSP_1	AE42	GPU_M_3_DQS_1_DN	GPU_M_3_DQS_1_DN	38
DDR3_DQSP_0	Y40	GPU_M_3_DQS_0_DP	GPU_M_3_DQS_0_DP	38
DDR3_DQSN_0	Y42	GPU_M_3_DQS_0_DN	GPU_M_3_DQS_0_DN	38
DDR2_DQSP_1	AE47	GPU_M_2_DQS_1_DP	GPU_M_2_DQS_1_DP	38
DDR2_DQSP_0	AE46	GPU_M_2_DQS_0_DP	GPU_M_2_DQS_0_DP	38
DDR2_DQSN_1	AE47	GPU_M_2_DQS_1_DN	GPU_M_2_DQS_1_DN	38
DDR2_DQSN_0	AE46	GPU_M_2_DQS_0_DN	GPU_M_2_DQS_0_DN	38
DDR1_DQSP_1	N36	GPU_M_1_DQS_1_DP	GPU_M_1_DQS_1_DP	37
DDR1_DQSP_0	N38	GPU_M_1_DQS_0_DP	GPU_M_1_DQS_0_DP	37
DDR1_DQSN_1	N31	GPU_M_1_DQS_1_DN	GPU_M_1_DQS_1_DN	37
DDR1_DQSN_0	N33	GPU_M_1_DQS_0_DN	GPU_M_1_DQS_0_DN	37
DDR0_DQSP_1	C42	GPU_M_0_DQS_1_DP	GPU_M_0_DQS_1_DP	37
DDR0_DQSP_0	D42	GPU_M_0_DQS_0_DP	GPU_M_0_DQS_0_DP	37
DDR0_DQSN_1	C38	GPU_M_0_DQS_1_DN	GPU_M_0_DQS_1_DN	37
DDR0_DQSN_0	D36	GPU_M_0_DQS_0_DN	GPU_M_0_DQS_0_DN	37
DDR1_CA0	G42	GPU_M_1_LP4X_CA_0	GPU_M_1_LP4X_CA_0	37
DDR1_CS0	G44	GPU_M_1_LP4X_CS_0	GPU_M_1_LP4X_CS_0	37
DDR1_CA4	K44	GPU_M_1_LP4X_CA_4	GPU_M_1_LP4X_CA_4	37
DDR1_CA3	N42	GPU_M_1_LP4X_CA_3	GPU_M_1_LP4X_CA_3	37
DDR1_CA2	N40	GPU_M_1_LP4X_CA_2	GPU_M_1_LP4X_CA_2	37
DDR1_CS1	G40	GPU_M_2_LP4X_CA_1	GPU_M_2_LP4X_CA_1	38
DDR2_CA1	T47	GPU_M_2_LP4X_CA_1	GPU_M_2_LP4X_CA_1	38
NC_6	Y40	GPU_M_3_LP4X_CA_1	GPU_M_3_LP4X_CA_1	38
DDR3_CA1	P47	GPU_M_2_LP4X_CA_0	GPU_M_2_LP4X_CA_0	38
DDR2_CA0	K46	GPU_M_0_LP4X_CA_2	GPU_M_0_LP4X_CA_2	37
DDR0_CA2	K47	GPU_M_0_LP4X_CA_4	GPU_M_0_LP4X_CA_4	37
DDR0_CA4	J50	GPU_M_0_LP4X_CA_3	GPU_M_0_LP4X_CA_3	37
DDR0_CA3	G50	GPU_M_0_LP4X_CA_5	GPU_M_0_LP4X_CA_5	37
DDR0_CA5	E49	GPU_M_0_LP4X_CS_0	GPU_M_0_LP4X_CS_0	37
DDR0_CS0	P46	GPU_M_3_LP4X_CS_0	GPU_M_3_LP4X_CS_0	38
DDR0_CS1	G49	GPU_M_3_LP4X_CS_0	GPU_M_3_LP4X_CS_0	38
DDR3_CS0	NC_7	GPU_M_2_LP4X_CA_2	GPU_M_2_LP4X_CA_2	38
NC_8	A47	GPU_M_2_LP4X_CA_3	GPU_M_2_LP4X_CA_3	38
DDR2_CA2	N43	GPU_M_1_LP4X_CA_5	GPU_M_1_LP4X_CA_5	37
DDR2_CA3	N44	GPU_M_3_LP4X_CA_0	GPU_M_3_LP4X_CA_0	38
DDR1_CA5	NC_9	GPU_M_1_LP4X_CA_5	GPU_M_1_LP4X_CA_5	37
DDR3_CA0	NC_10	GPU_M_3_LP4X_CA_0	GPU_M_3_LP4X_CA_0	38
DDR2_CS1	Y46	GPU_DDR0_ALERT_N	GPU_DDR0_ALERT_N	38
DDR3_CS1	Y40	GPU_DDR0_ALERT_N	GPU_DDR0_ALERT_N	38
DDR0_ALERT	AA46	GPU_DRAM_RESET_N	GPU_DRAM_RESET_N	38
DDR0_VREF_CA	BK8	GPU_DRAM_RESET_N	GPU_DRAM_RESET_N	38
DDR0_DRAM_RESET	NC_11	GPU_DRAM_RESET_N	GPU_DRAM_RESET_N	38
DDR_VTT_CTL	C47	GPU_DDR_COMP_0	GPU_DDR_COMP_0	38
DDR_RCOMP	B46	GPU_DDR_COMP_0	GPU_DDR_COMP_0	38





8 of 14

UG4H		
A12	VSS_001	AL49
A16	VSS_002	AM36
A21	VSS_003	AM39
A25	VSS_004	AM4
A29	VSS_005	AM45
A33	VSS_006	AM49
A36	VSS_007	AN39
A42	VSS_008	AN40
A44	VSS_009	AN42
A46	VSS_010	AN44
A5	VSS_011	AN45
A7	VSS_012	AN46
AA13	VSS_013	AN47
AA39	VSS_014	AN48
AA45	VSS_015	AN49
AA49	VSS_016	AP1
AB39	VSS_017	AP2
AB40	VSS_018	AP5
AB42	VSS_019	AP6
AB43	VSS_020	AP7
AB44	VSS_021	AP8
AB45	VSS_022	AP9
AB46	VSS_023	AR10
AB49	VSS_024	AR39
AD1	VSS_025	AR4
AD2	VSS_026	AR45
AD36	VSS_027	AR7
AD39	VSS_028	AR8
AD4	VSS_029	AT36
AD41	VSS_030	AT39
AD43	VSS_031	AT43
AD5	VSS_032	AT44
AD6	VSS_033	AT45
AD7	VSS_034	AT46
AE11	VSS_035	AU39
AE39	VSS_036	AU4
AE4	VSS_037	AU45
AE43	VSS_038	AU49
AE44	VSS_039	AU7
AE45	VSS_040	AW11
AE49	VSS_041	AW13
AE7	VSS_042	AW39
AF39	VSS_043	AW4
AF45	VSS_044	AW40
AF49	VSS_045	AW42
AG4	VSS_046	AW43
AG7	VSS_047	AW44
AH39	VSS_048	AW45
AH40	VSS_049	AW46
AH42	VSS_050	AW47
AH43	VSS_051	AW49
AH44	VSS_052	AY36
AH45	VSS_053	AY39
AH46	VSS_054	AY4
AH47	VSS_055	AY45
AH49	VSS_056	AY7
AJ39	VSS_057	B13
AJ4	VSS_058	B18
AJ45	VSS_059	B19
AJ7	VSS_060	B22
AK11	VSS_061	B26
AK13	VSS_062	B29
AK4	VSS_063	B33
AK7	VSS_064	B36
AL39	VSS_065	B39
AL43	VSS_066	B42
AL44	VSS_067	B47
AL45	VSS_068	B48
	VSS_069	B49
	VSS_070	B49

DG1_GPU_IP_EXT
DG1_GPU

9 of 14

UG4I		
B9	VSS_141	BK45
BA39	VSS_142	BK46
BA43	VSS_143	BK47
BA44	VSS_144	BK49
BA45	VSS_145	BL25
BA49	VSS_146	BL29
BB12	VSS_147	BL34
BB4	VSS_148	BL39
BB7	VSS_149	BL45
BC39	VSS_150	BL5
BC45	VSS_151	BM1
BC49	VSS_152	BM10
BD1	VSS_153	BM12
BD11	VSS_154	BM29
BD2	VSS_155	BM3
BD39	VSS_156	BM32
BD4	VSS_157	BM34
BD40	VSS_158	BM36
BD43	VSS_159	BM38
BD44	VSS_160	BM39
BD45	VSS_161	BM43
BD49	VSS_162	BM44
BD49	VSS_163	BM45
BD49	VSS_164	BM49
BD5	VSS_165	BN15
BD6	VSS_166	BN17
BD7	VSS_167	BN19
BE10	VSS_168	BN20
BE10	VSS_169	BN22
BE39	VSS_170	BN24
BE43	VSS_171	BN27
BF14	VSS_172	BN29
BF14	VSS_173	BN34
BF24	VSS_174	BN6
BG1	VSS_175	BP14
BG11	VSS_176	BP19
BG39	VSS_177	BP22
BG39	VSS_178	BP25
BG39	VSS_179	BP29
BG39	VSS_180	BP34
BG39	VSS_181	BP39
BG39	VSS_182	BP4
BG39	VSS_183	BP45
BG43	VSS_184	BP49
BG43	VSS_185	BR1
BG45	VSS_186	BR40
BG45	VSS_187	BR42
BH15	VSS_188	BR43
BH17	VSS_189	BR46
BH19	VSS_190	BR47
BH22	VSS_191	BR50
BH24	VSS_192	BT12
BH25	VSS_193	BT15
BH29	VSS_194	BT30
BH34	VSS_195	BT32
BH34	VSS_196	BT33
BH39	VSS_197	BT36
BH45	VSS_198	BT38
BH49	VSS_199	BT39
BH7	VSS_200	BT9
BJ34	VSS_201	BU1
BJ39	VSS_202	BU15
BK2	VSS_203	BU17
BK39	VSS_204	BU20
BK43	VSS_205	BU24
BK43	VSS_206	BU27
BK43	VSS_207	
BK43	VSS_208	
BK43	VSS_209	
BK43	VSS_210	

DG1_GPU_IP_EXT
DG1_GPU

10 of 14

UG4J		
BU39	VSS_281	E46
BU39	VSS_282	E47
BU39	VSS_283	E50
BU4	VSS_284	F12
BU45	VSS_285	F16
BU47	VSS_286	F21
BU49	VSS_287	F29
BU50	VSS_288	F31
BU6	VSS_289	F33
BU1	VSS_290	F34
BU11	VSS_291	F36
BU14	VSS_292	F37
BU15	VSS_293	F39
BU17	VSS_294	F4
BU19	VSS_295	F40
BU20	VSS_296	F42
BU22	VSS_297	F44
BU24	VSS_298	F45
BU25	VSS_299	F50
BU29	VSS_300	F54
BU29	VSS_301	F58
BU30	VSS_302	F61
BU30	VSS_303	G13
BU30	VSS_304	G18
BU32	VSS_305	G22
BU33	VSS_306	G26
BU39	VSS_307	G29
BU45	VSS_308	G34
BU48	VSS_309	G39
BU5	VSS_310	G45
BU50	VSS_311	G49
BU12	VSS_312	G5
BU15	VSS_313	G5
BU3	VSS_314	G59
BU30	VSS_315	G61
BU39	VSS_316	G63
BU39	VSS_317	G64
BU39	VSS_318	G66
BU39	VSS_319	G68
BU39	VSS_320	G69
BU4	VSS_321	G73
BU45	VSS_322	G74
BU45	VSS_323	G75
BU45	VSS_324	G76
BU45	VSS_325	G77
BU45	VSS_326	G78
BU45	VSS_327	G79
BU45	VSS_328	G82
BU45	VSS_329	G83
BU45	VSS_330	G89
BU45	VSS_331	G90
BU45	VSS_332	G91
BU45	VSS_333	G93
BU45	VSS_334	G94
BU45	VSS_335	G95
BU45	VSS_336	G96
BU45	VSS_337	G97
BU45	VSS_338	G98
BU45	VSS_339	G99
BU45	VSS_340	G100
BU45	VSS_341	G101
BU45	VSS_342	G102
BU45	VSS_343	G103
BU45	VSS_344	G104
BU45	VSS_345	G105
BU45	VSS_346	G106
BU45	VSS_347	G107
BU45	VSS_348	G108
BU45	VSS_349	G109
BU45	VSS_350	G110

DG1_GPU_IP_EXT
DG1_GPU

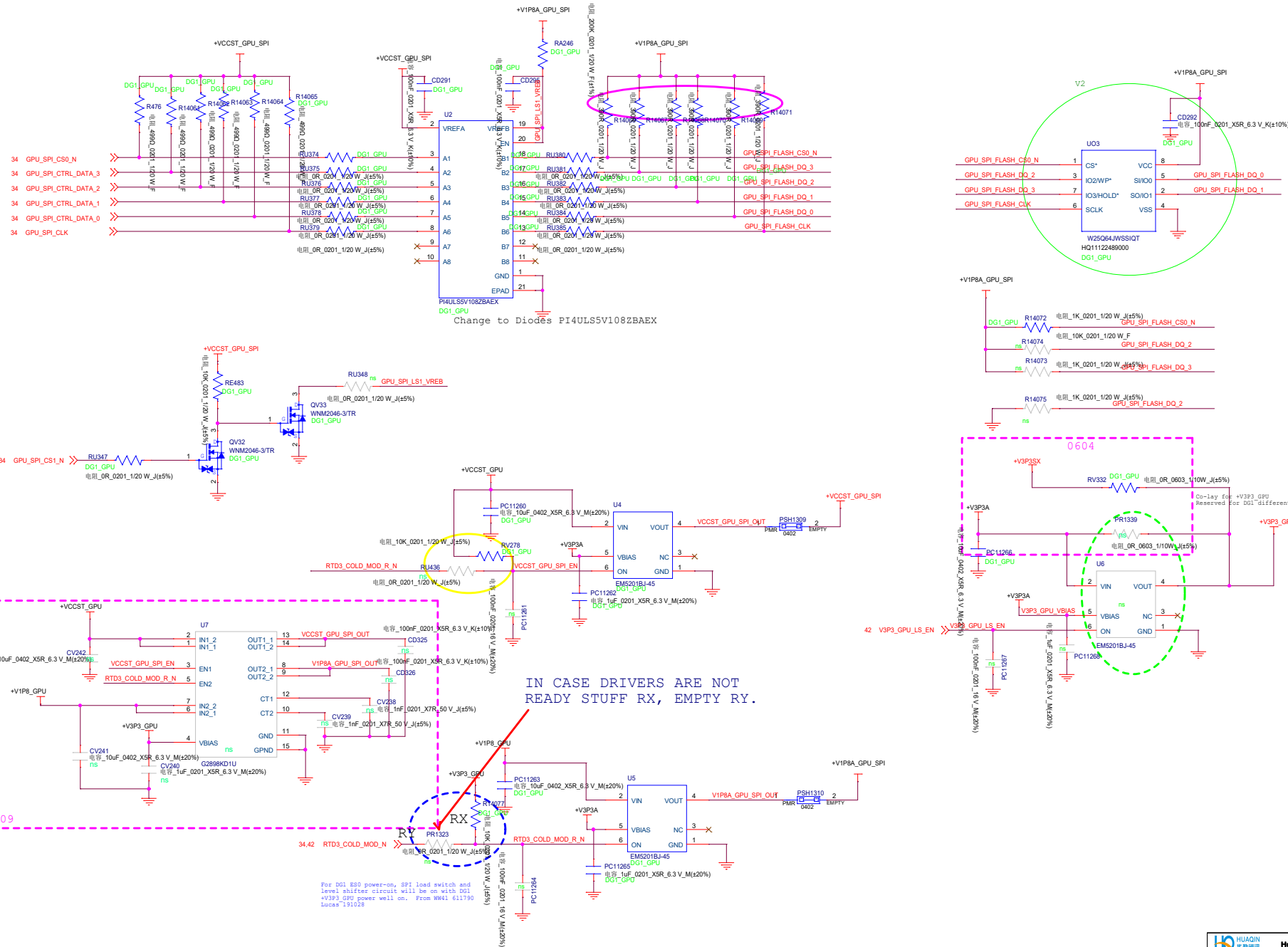
11 of 14

UG4K		
M1	VSS_421	T38
M11	VSS_422	T39
M19	VSS_423	T45
N34	VSS_424	T49
N39	VSS_425	T53
N45	VSS_426	T54
P12	VSS_427	T55
P31	VSS_428	T56
P33	VSS_429	T57
P36	VSS_430	T58
P39	VSS_431	T59
P43	VSS_432	T60
P44	VSS_433	T61
P45	VSS_434	T62
P49	VSS_435	T63
P7	VSS_436	T64
R1	VSS_437	T65
R13	VSS_438	T66
R18	VSS_439	T67
R22	VSS_440	T68
R26	VSS_441	T69
R6	VSS_442	T70
T18	VSS_443	T71
T2	VSS_444	T72
T26	VSS_445	T73
T26	VSS_446	T74
T26	VSS_447	T75
T26	VSS_448	T76

DG1_GPU_IP_EXT
DG1_GPU

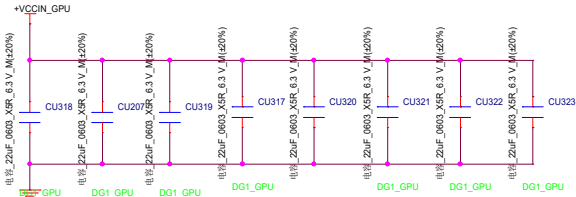


FLASH

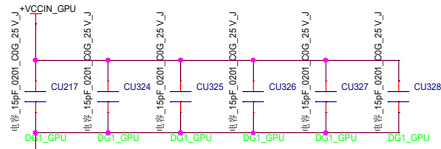


+VCCIN_GPU

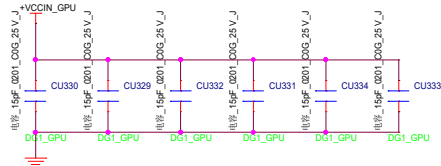
TOP



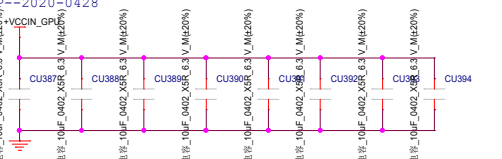
TOP -15PF X6



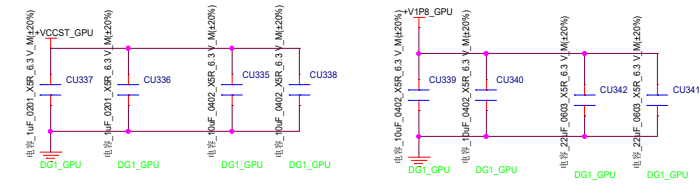
BOTTOM -15PF X6



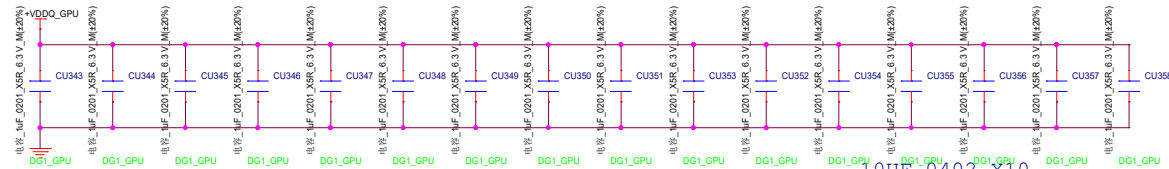
TOP--2020-0428



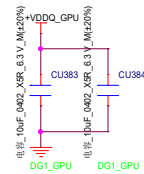
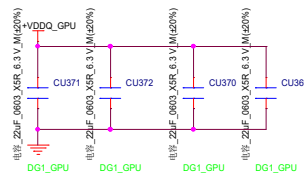
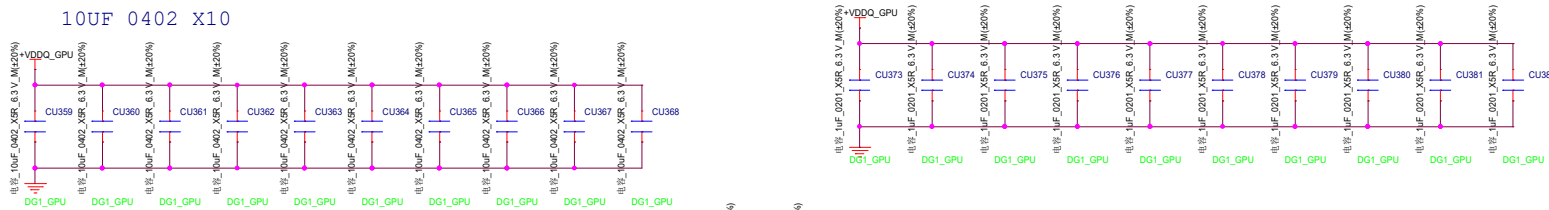
PLACE AS CLOSE AS POSSIBLE TO THE SOC

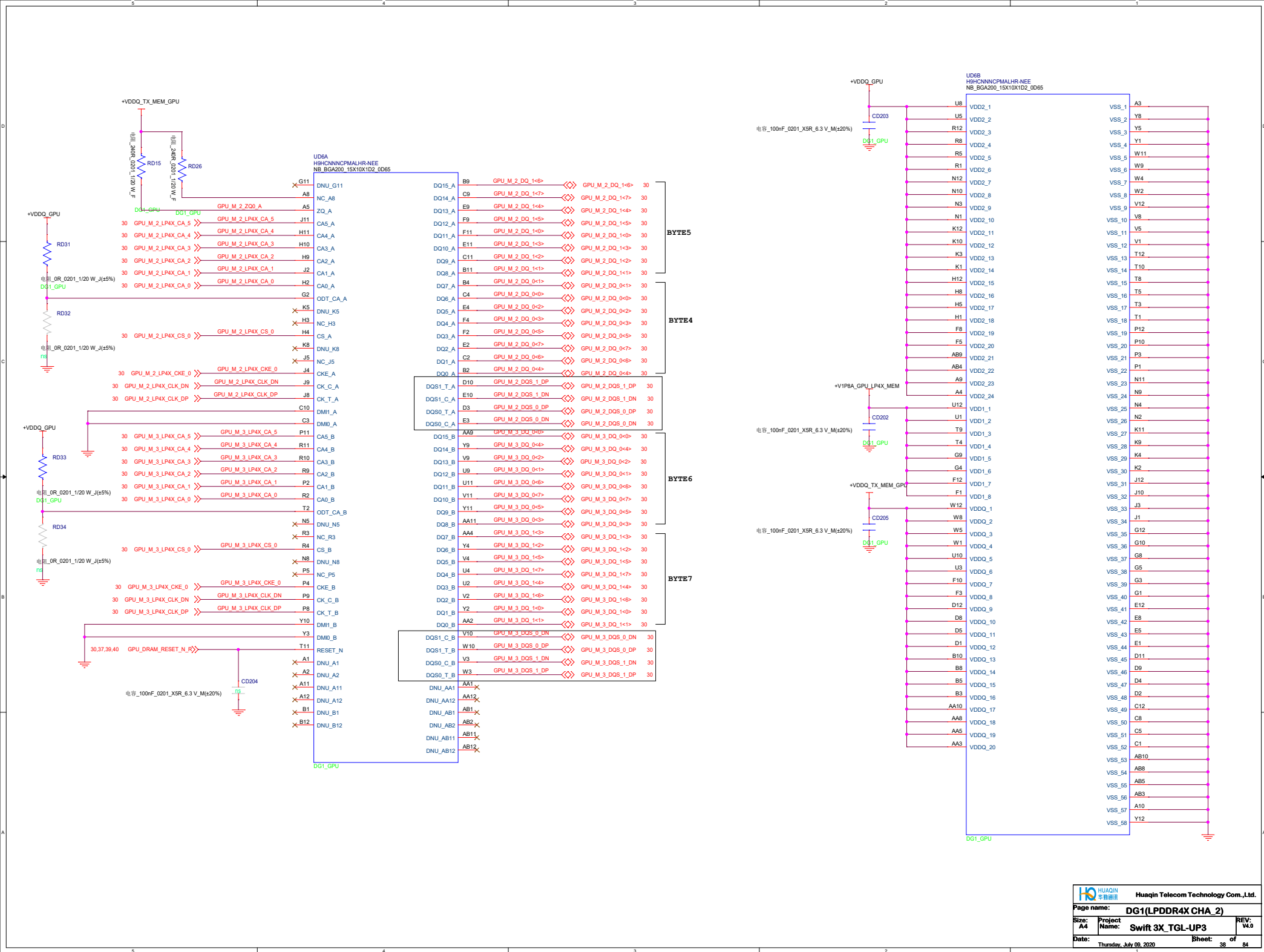


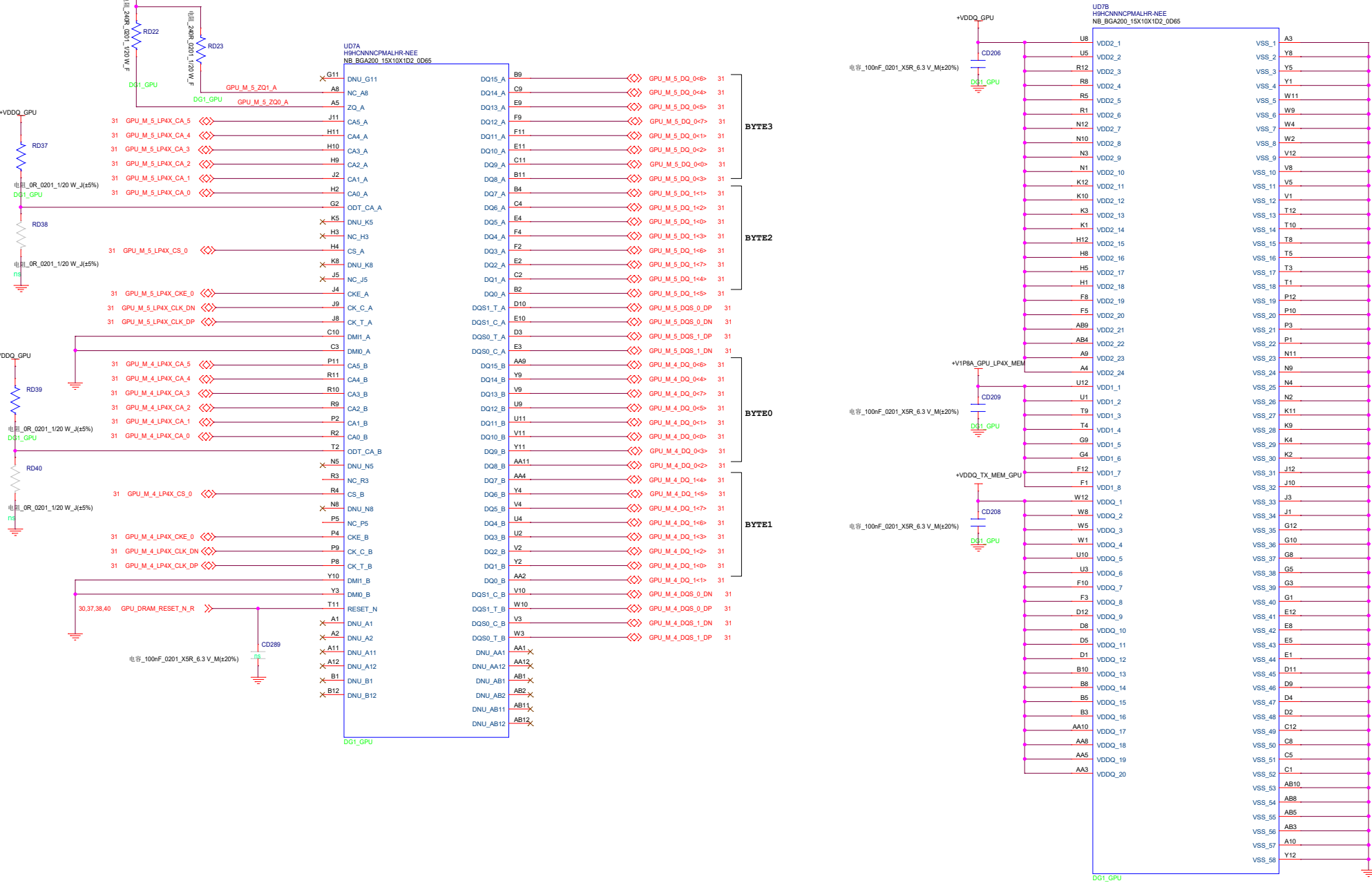
1UF 0201 X16



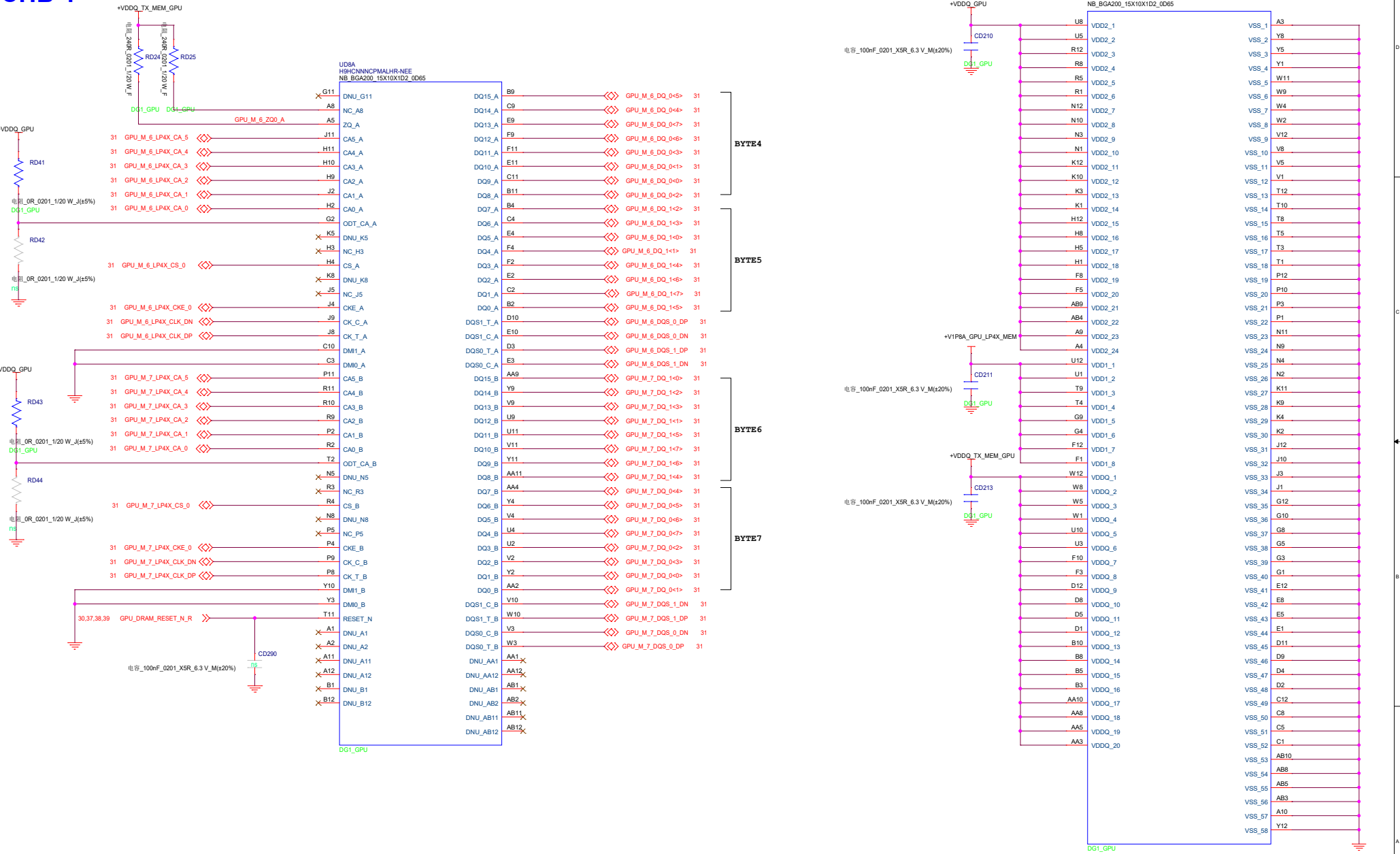
100UF 0402 X10



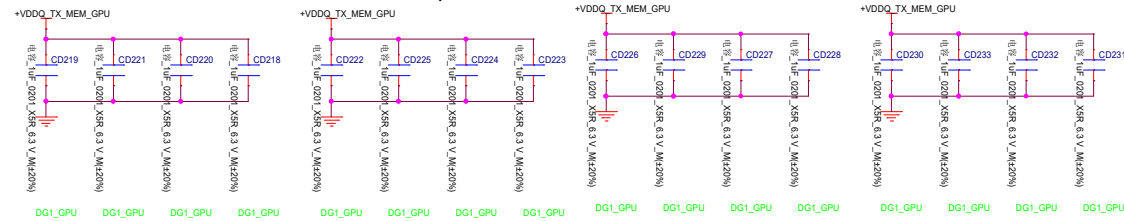




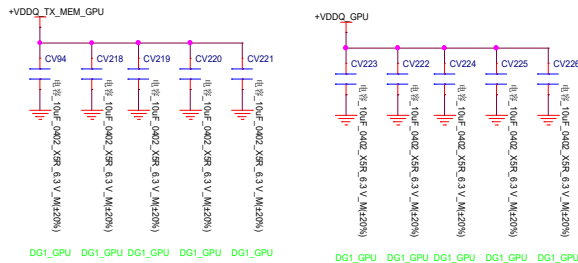
CHB-1



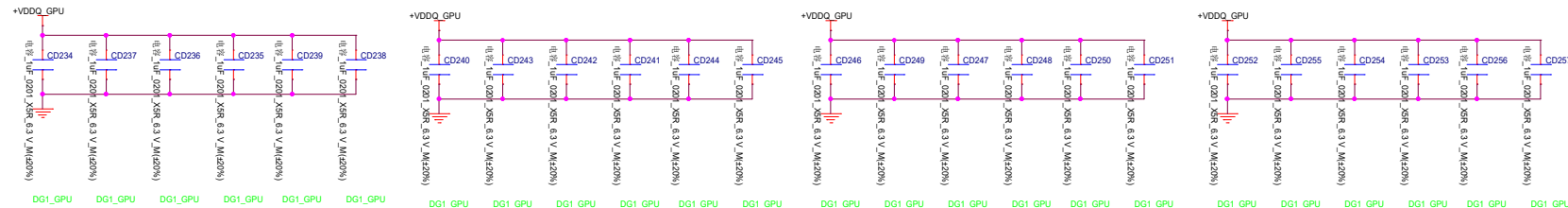
4 CAPS PER LPDDR4X, 2 CAPS PER SHORT EDGE



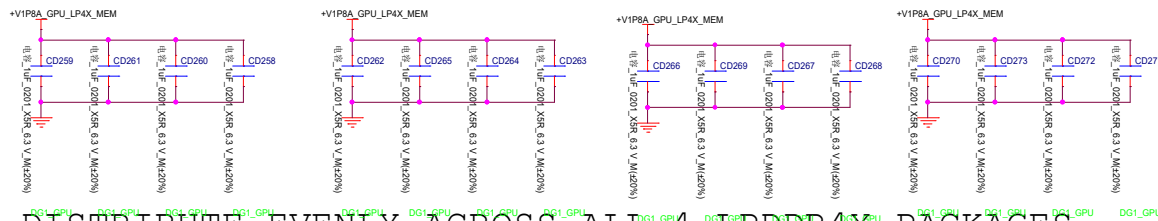
DISTRIBUTE EVENLY FOR ALL LPDDR4X PACKAGES



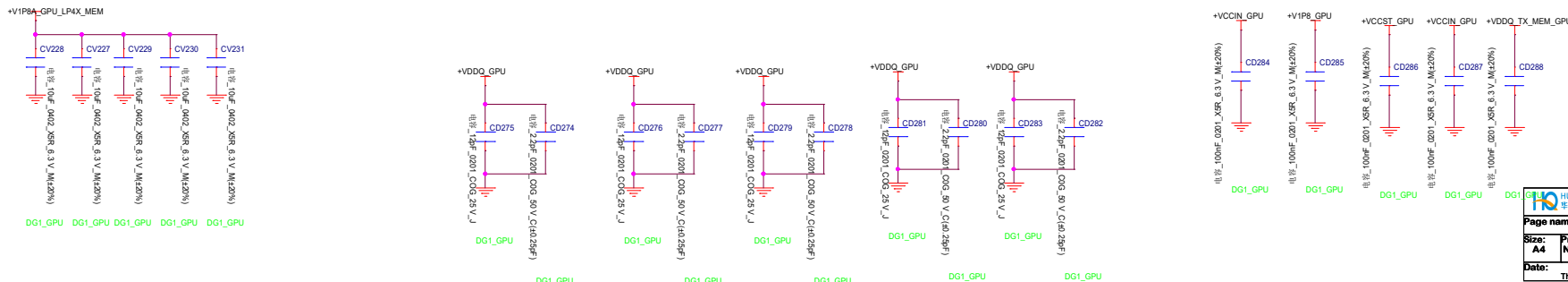
DISTRIBUTE 6 CAPS AROUND EACH LPDDR4X PACKAGE 1 CAP PER SHORT EDGE 2 CAPS PER LONG EDGE

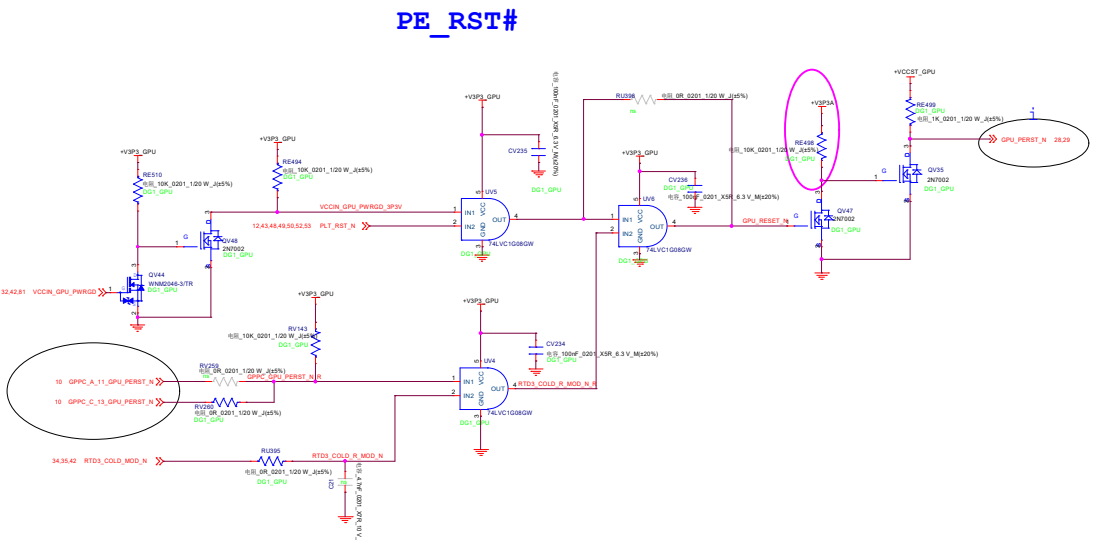
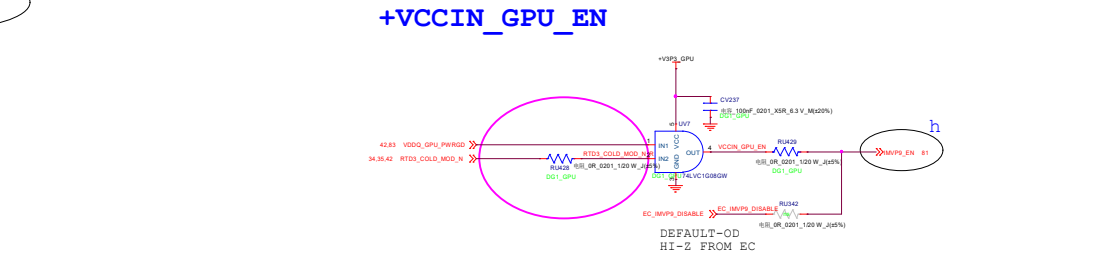
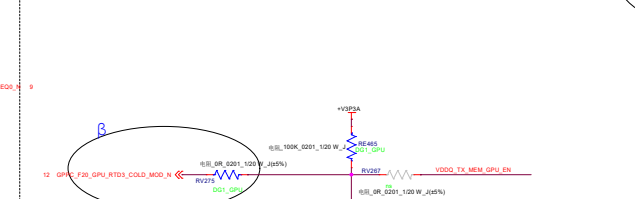
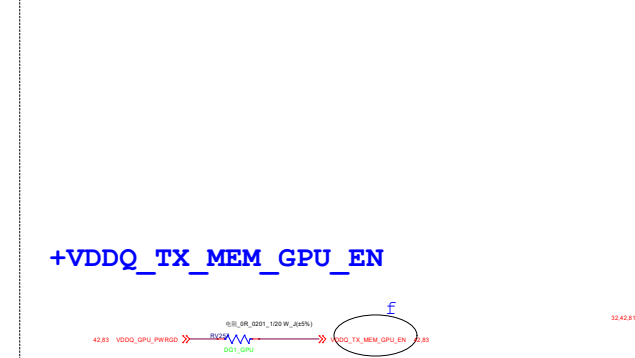
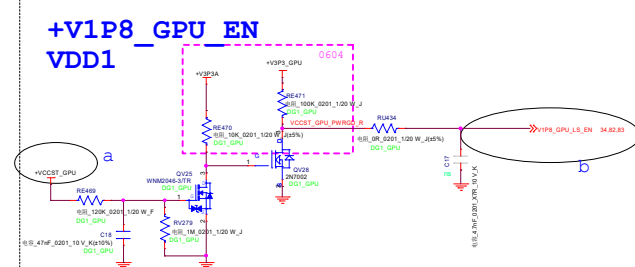
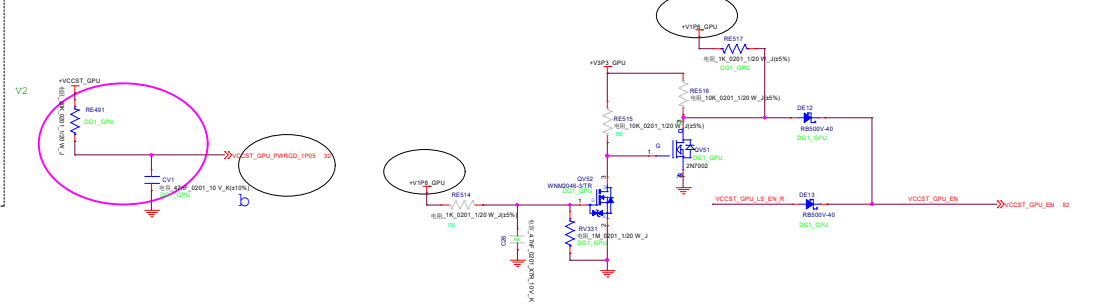


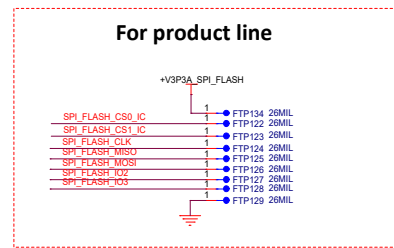
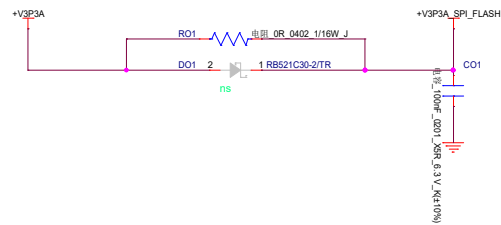
4 CAPS PER LPDDR4X, 2 CAPS PER SHORT EDGE



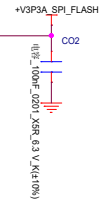
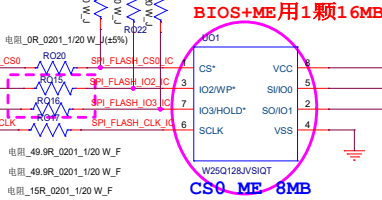
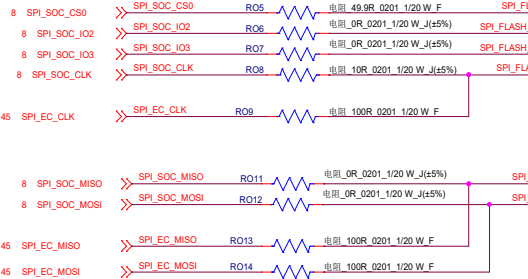
DISTRIBUTE EVENLY ACROSS ALL 4 LPDDR4X PACKAGES



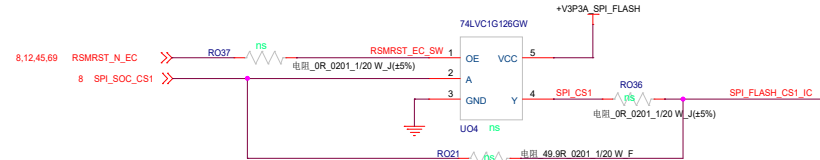
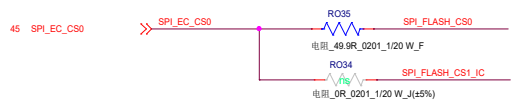
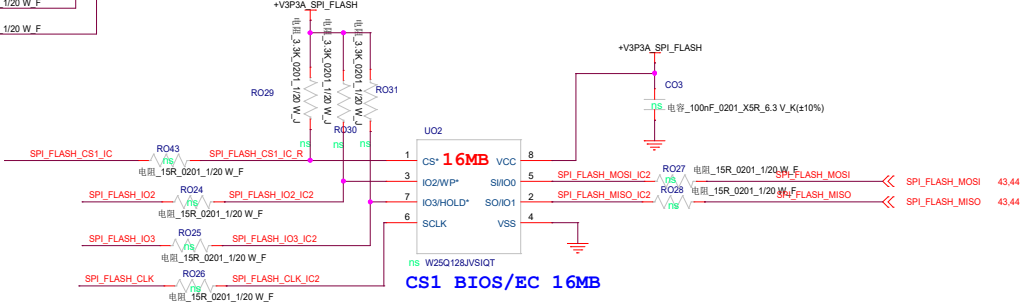
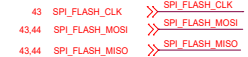


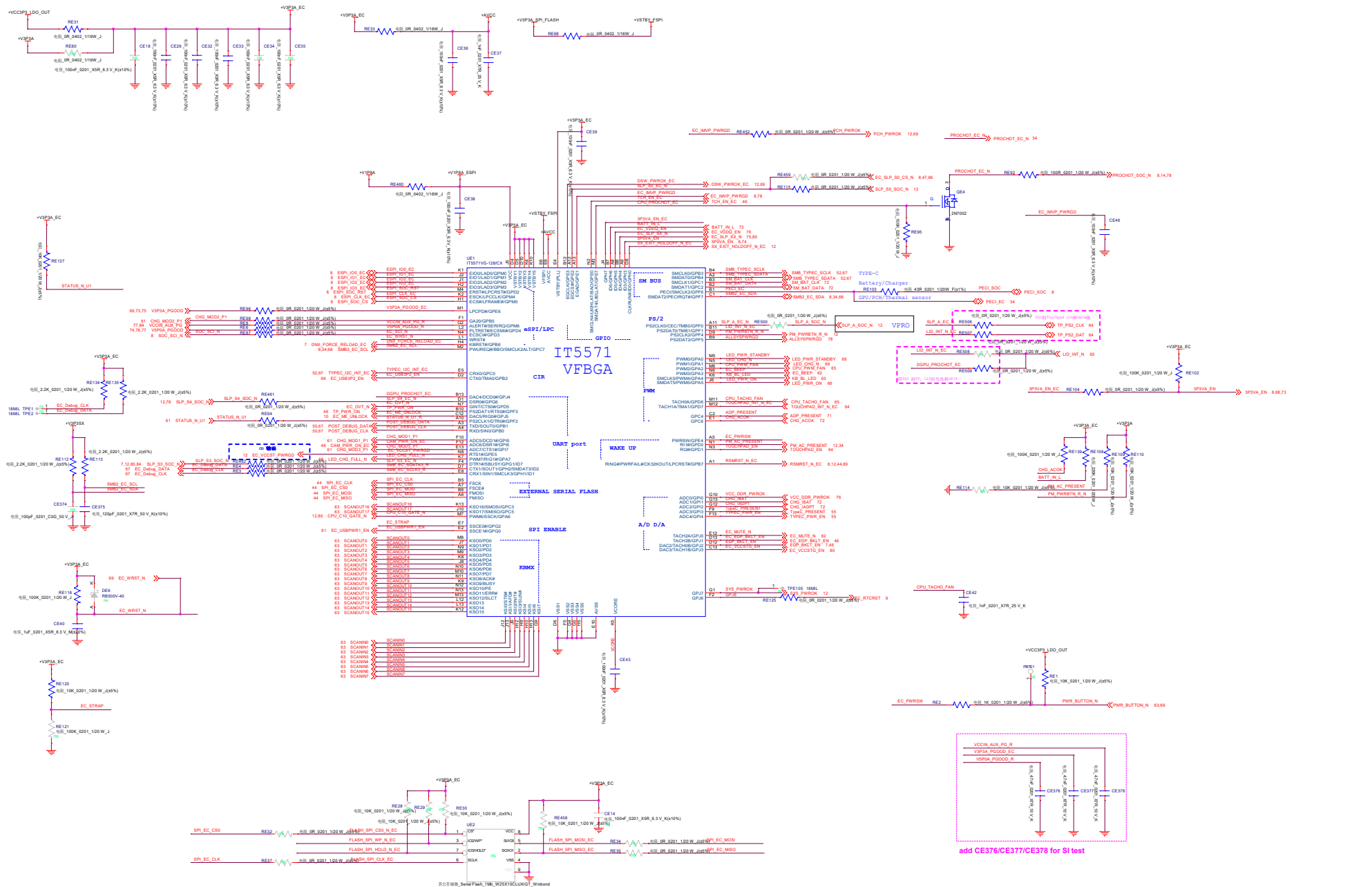


Series RO5,RO6,RO7,RO8 ,RO11,RO12place Close to PCH <1000MIL,
Series RO9,RO13,RO14place Close to EC <1000MIL,
Series RO20,RO15,RO16,RO17,RO18,RO19place Close to UO1<1000MIL,
Series RO43,RO24,RO25,RO26,RO27,RO28place Close to UO2<1000MIL,



Distinguish 2 16MB ROM.
SMT BOM must add 2 different HQ code.

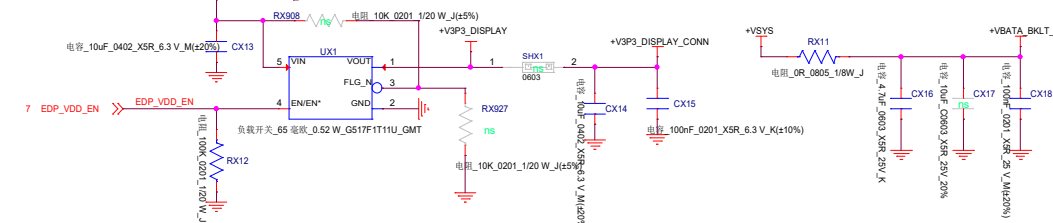




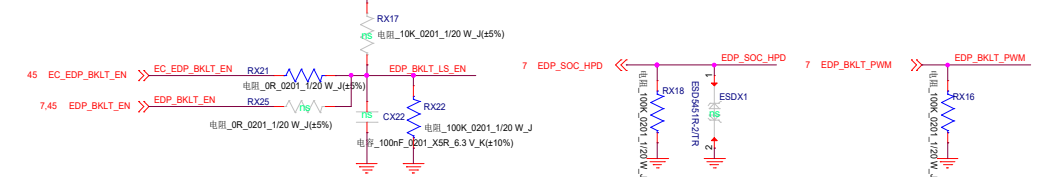
eDP Signal



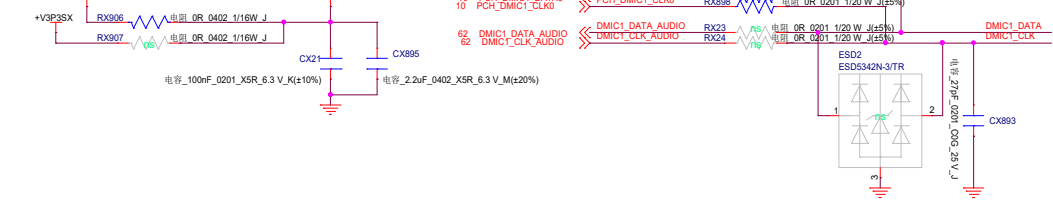
eDP VCC & BL Power



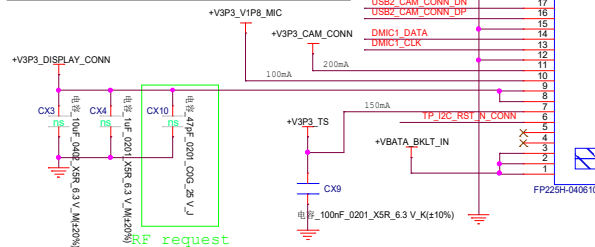
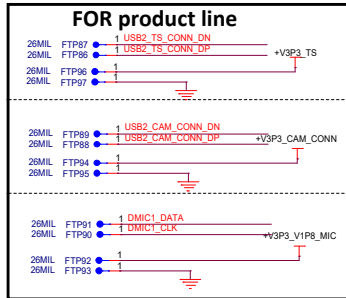
eDP Control



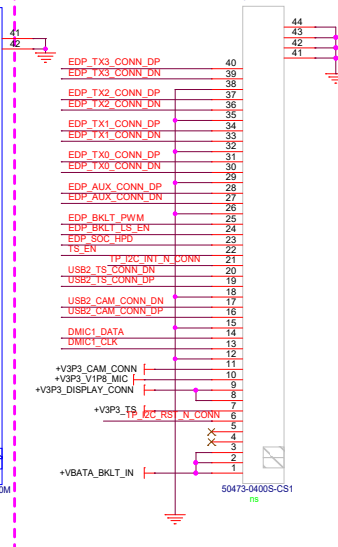
MIC



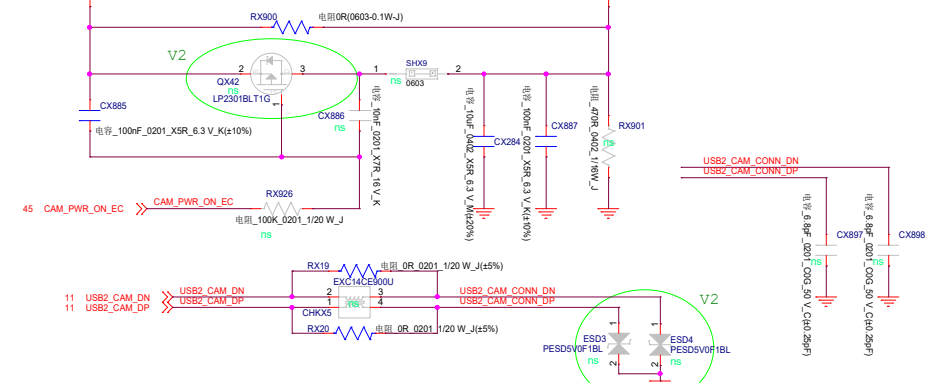
eDP & CAM & DMIC & Touch Panel CONN



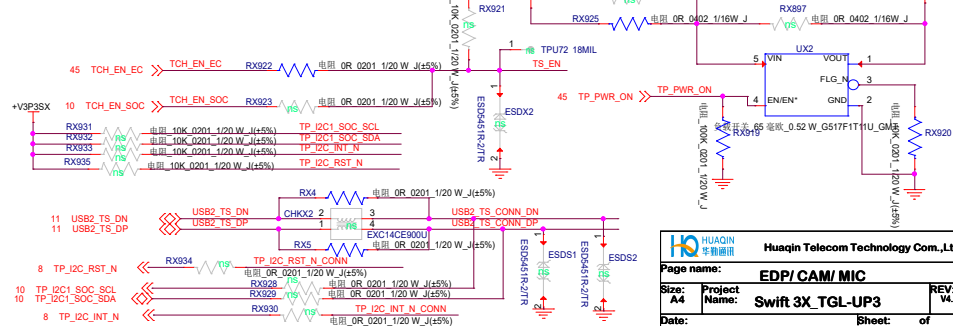
Reserve for 4K panel Conn need create symbol and footprint



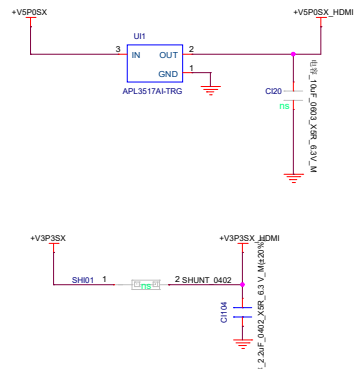
CAM Power



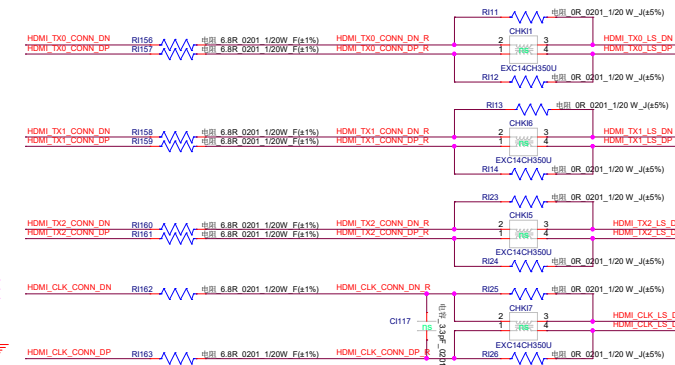
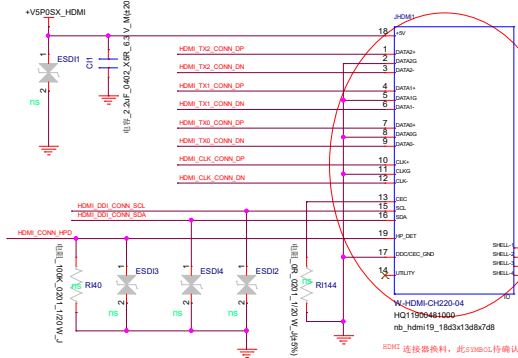
Touch Panel



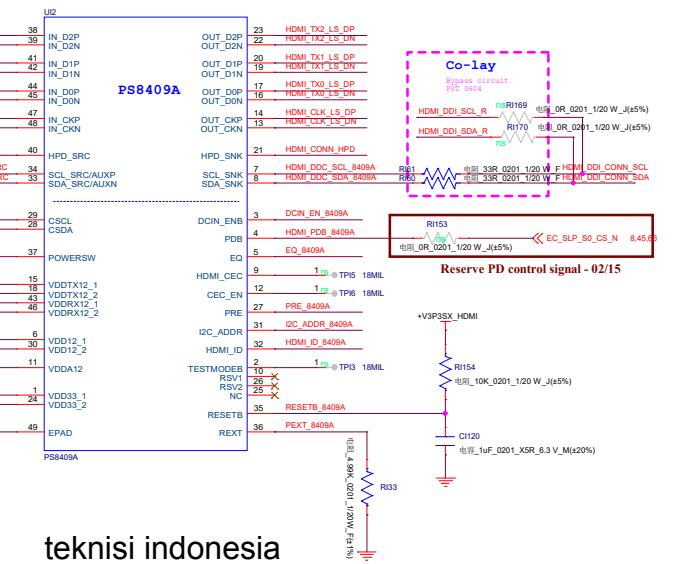
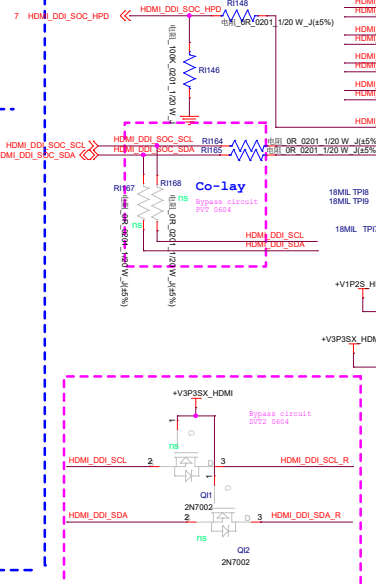
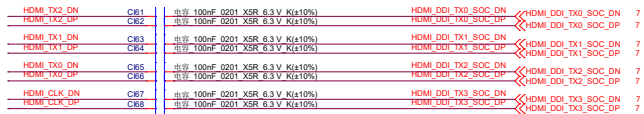
Power 1



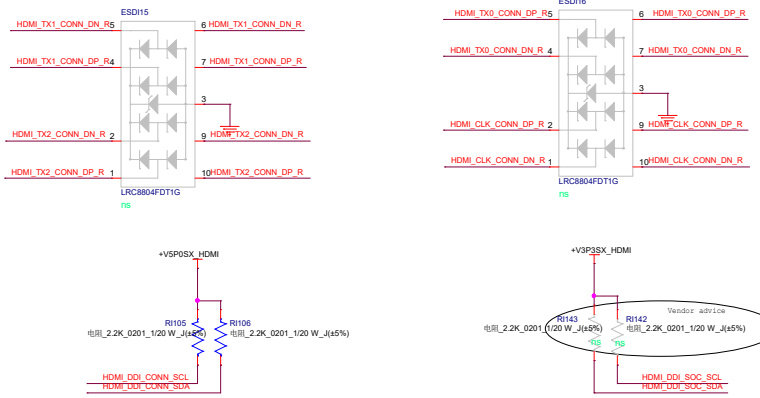
HDMI CONN



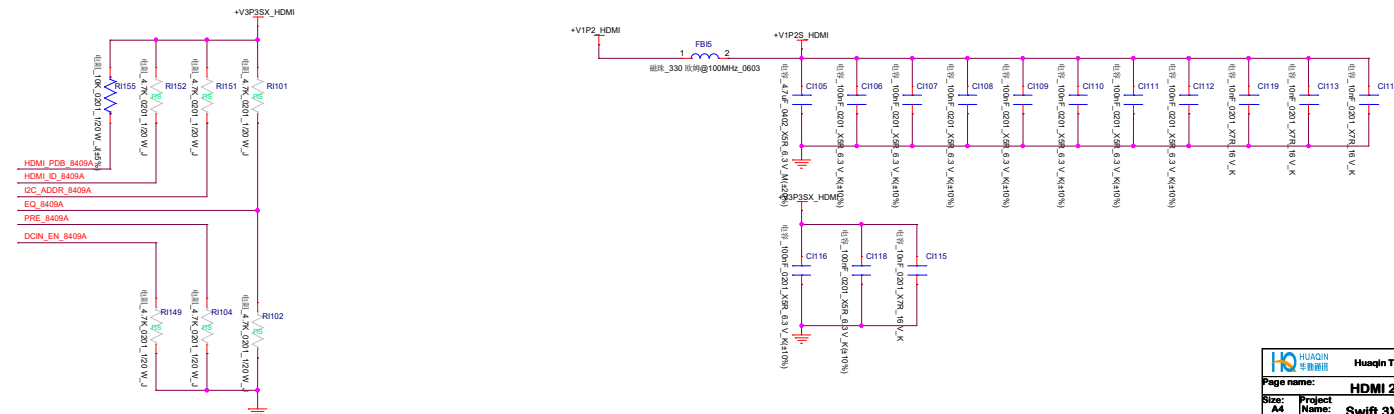
Signal



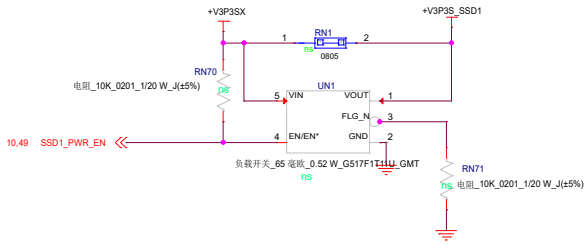
ESD



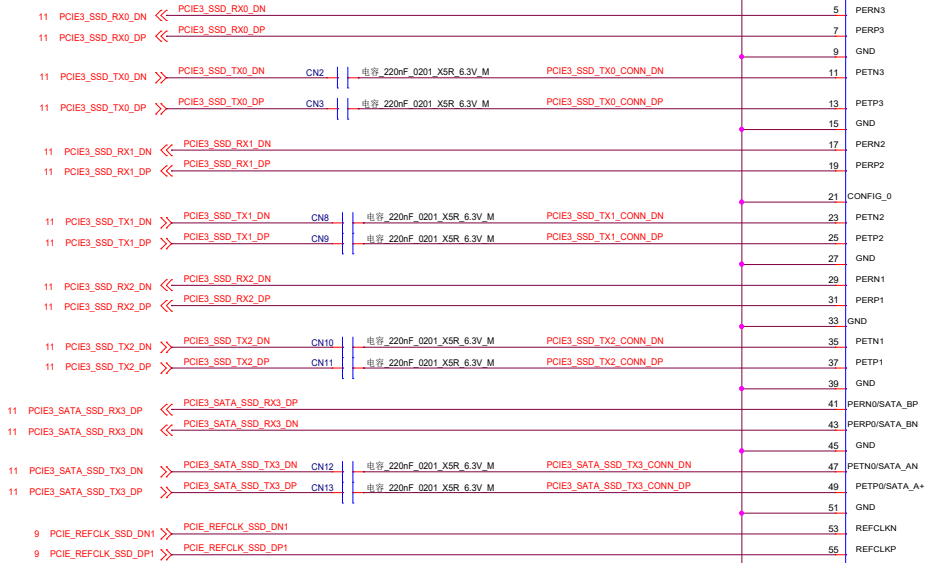
teknisi indonesia



SSD



V2

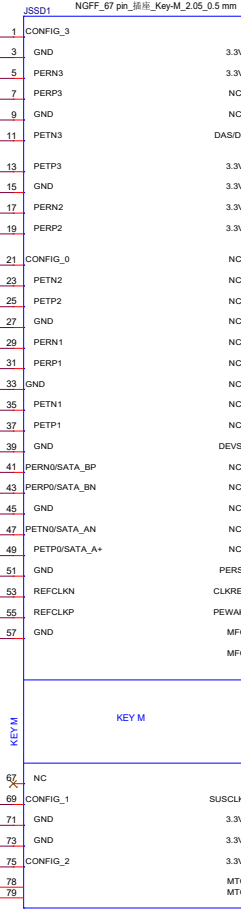


11 SSD1_DET to SSD1_DET

MS 需要同时接到CPU GPIO

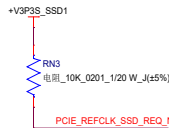
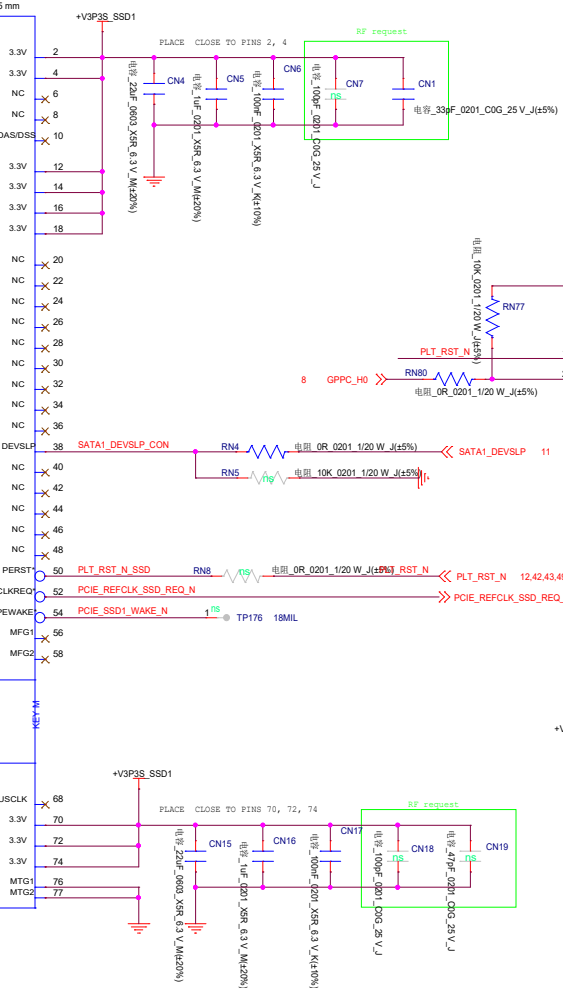


SATA - GND; PCIE - NC

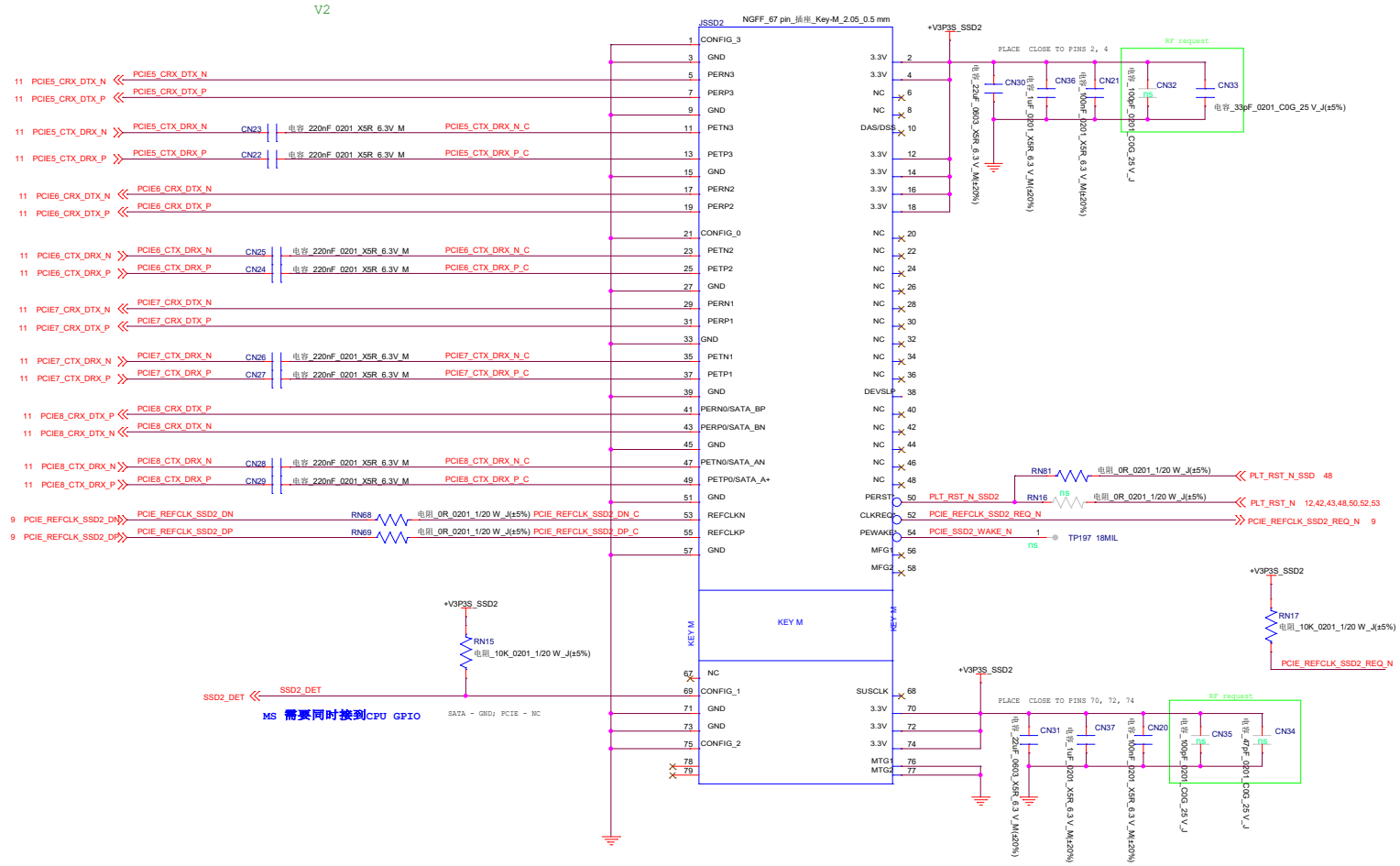
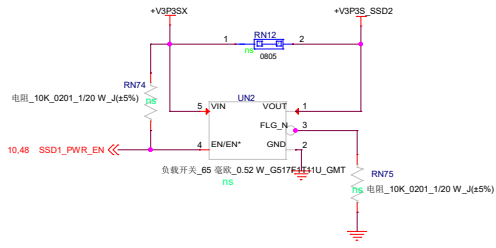


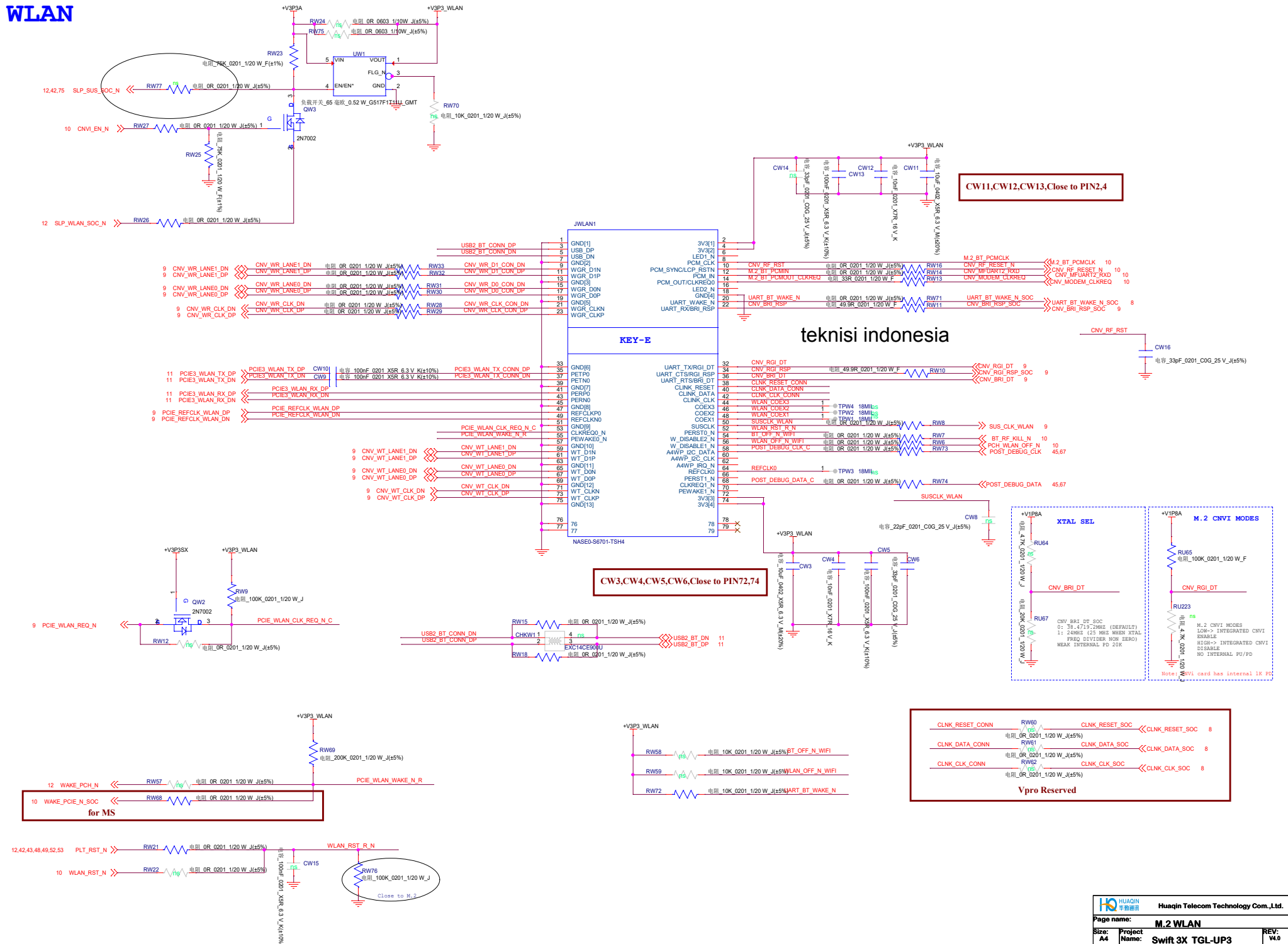
KEY M

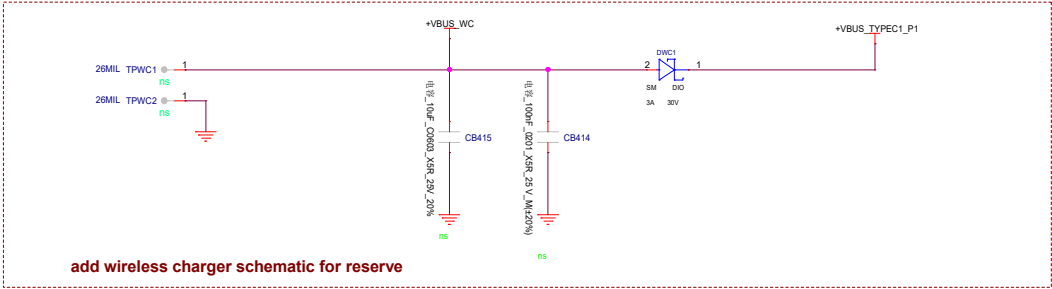
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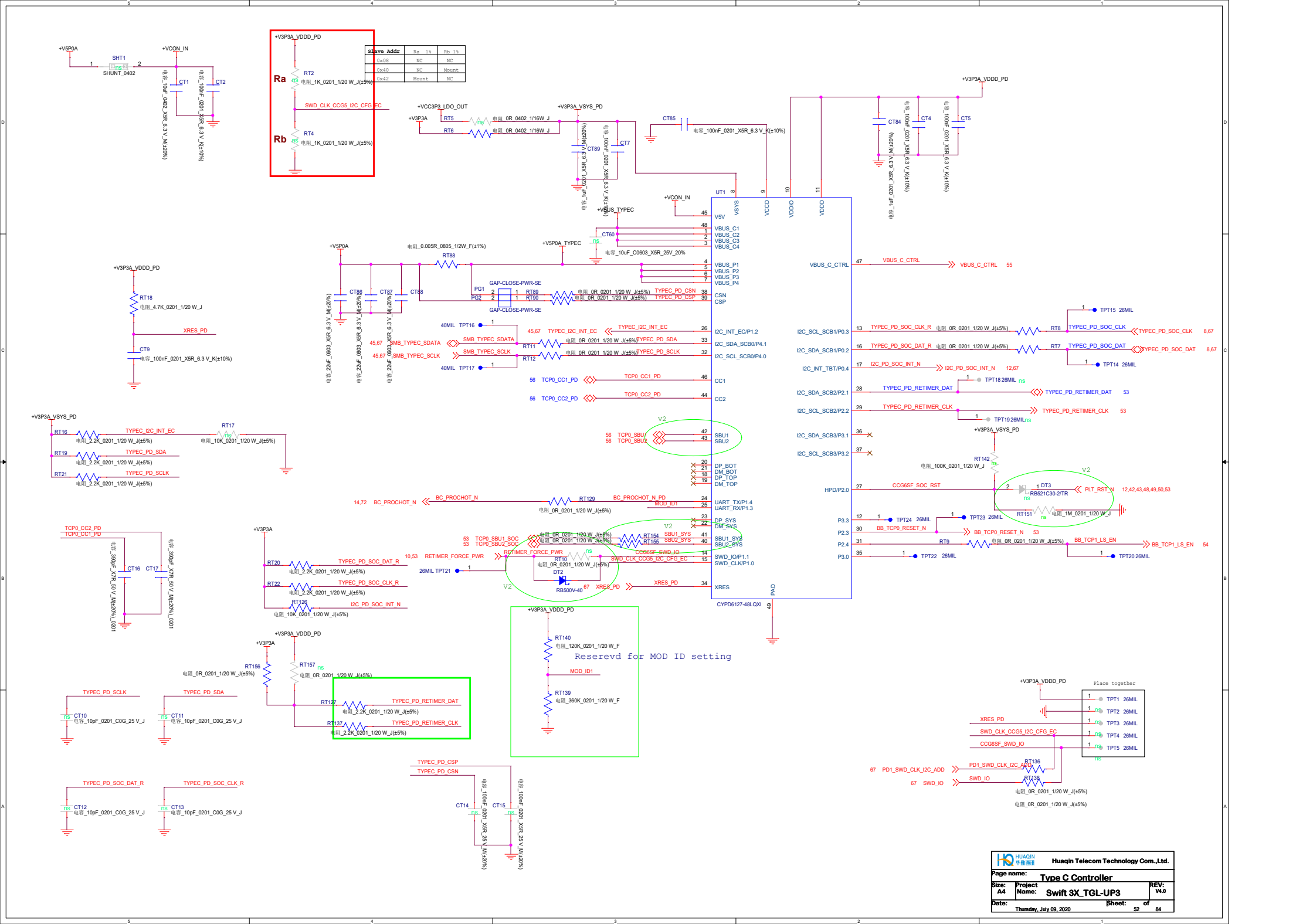


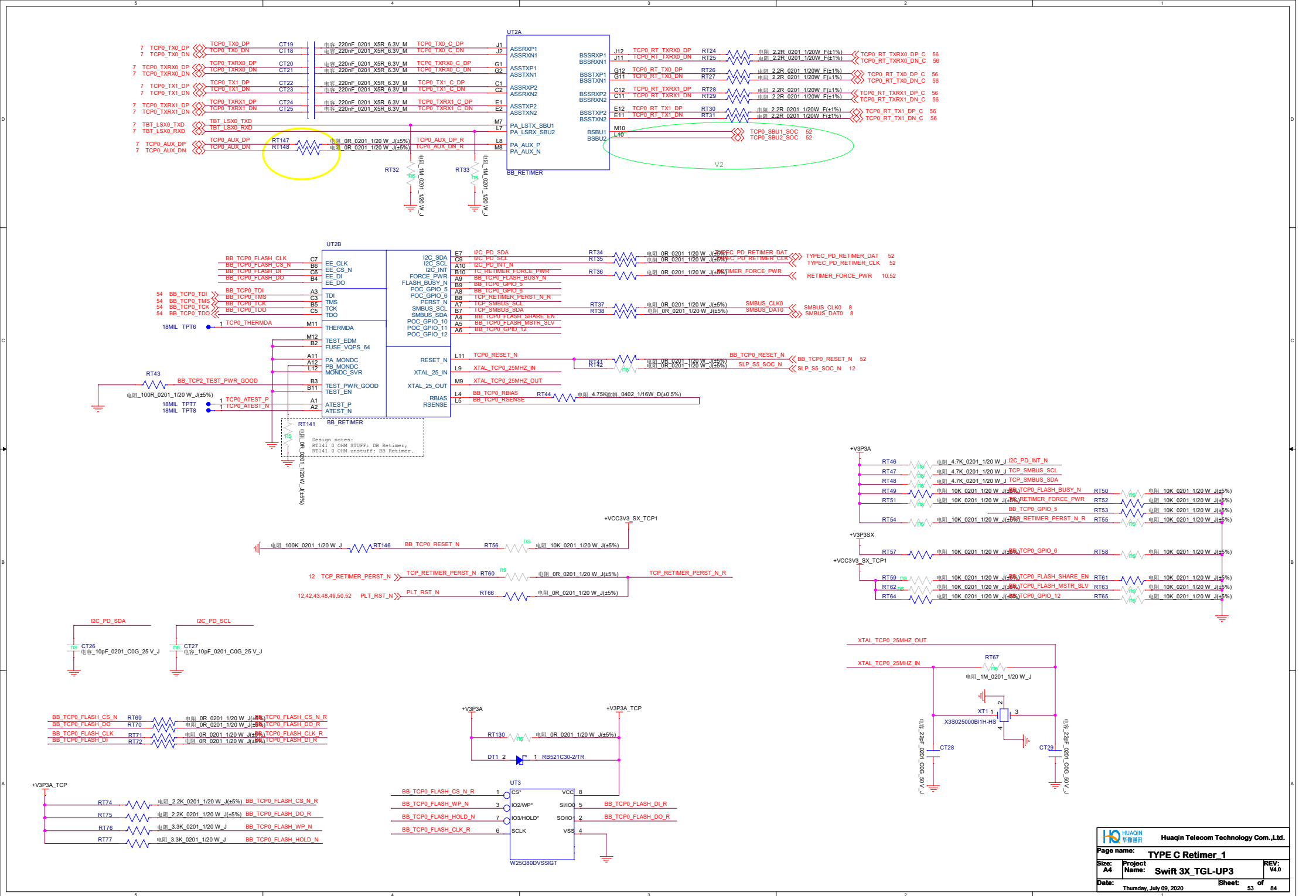
SSD2

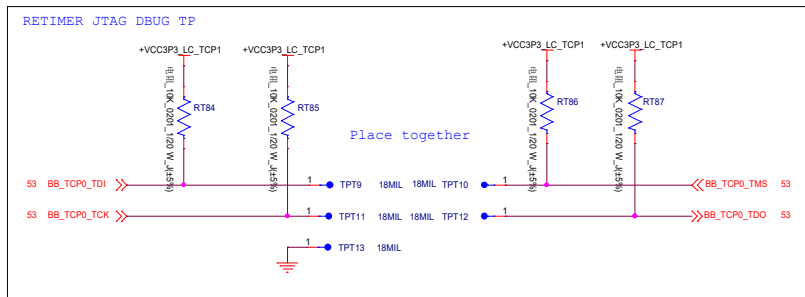
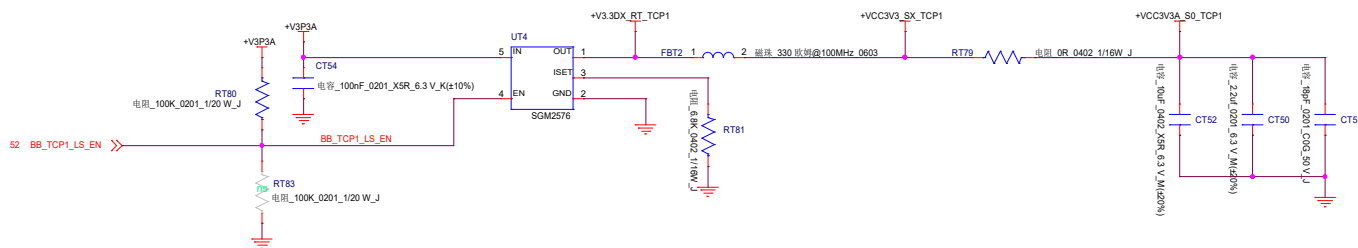
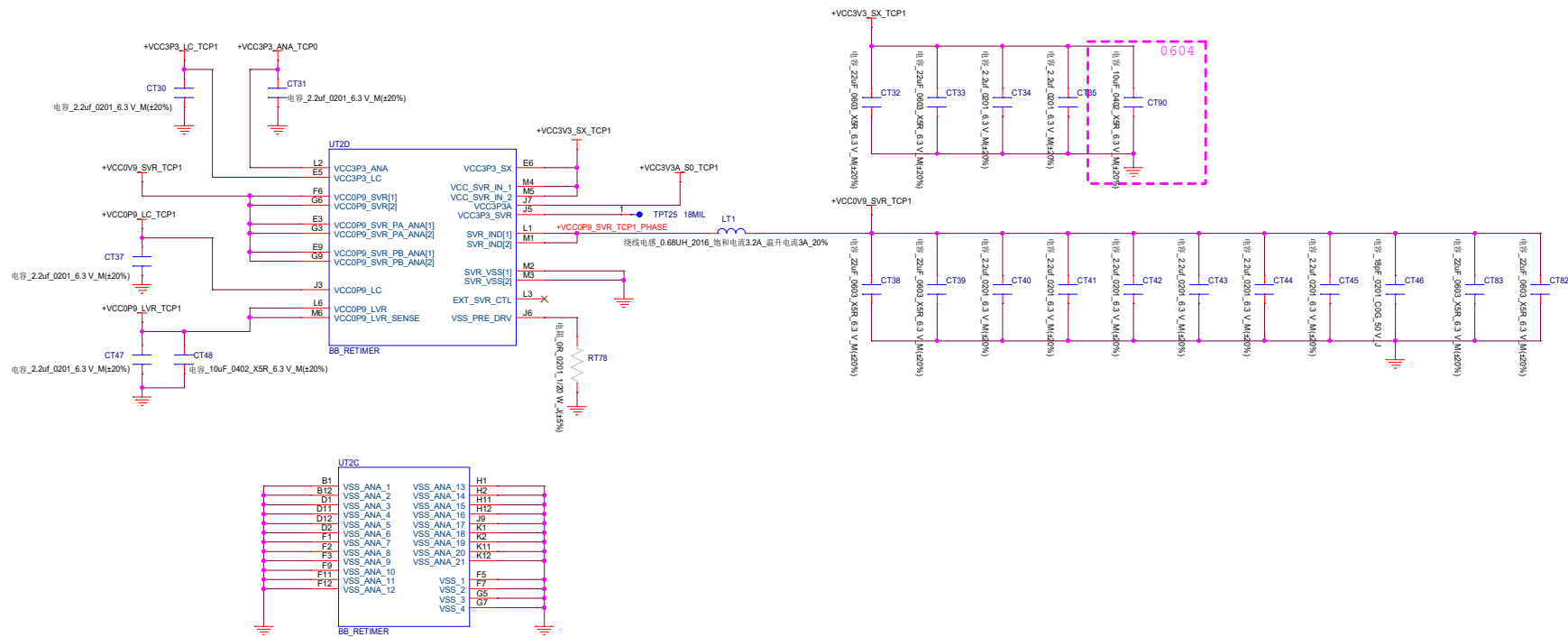






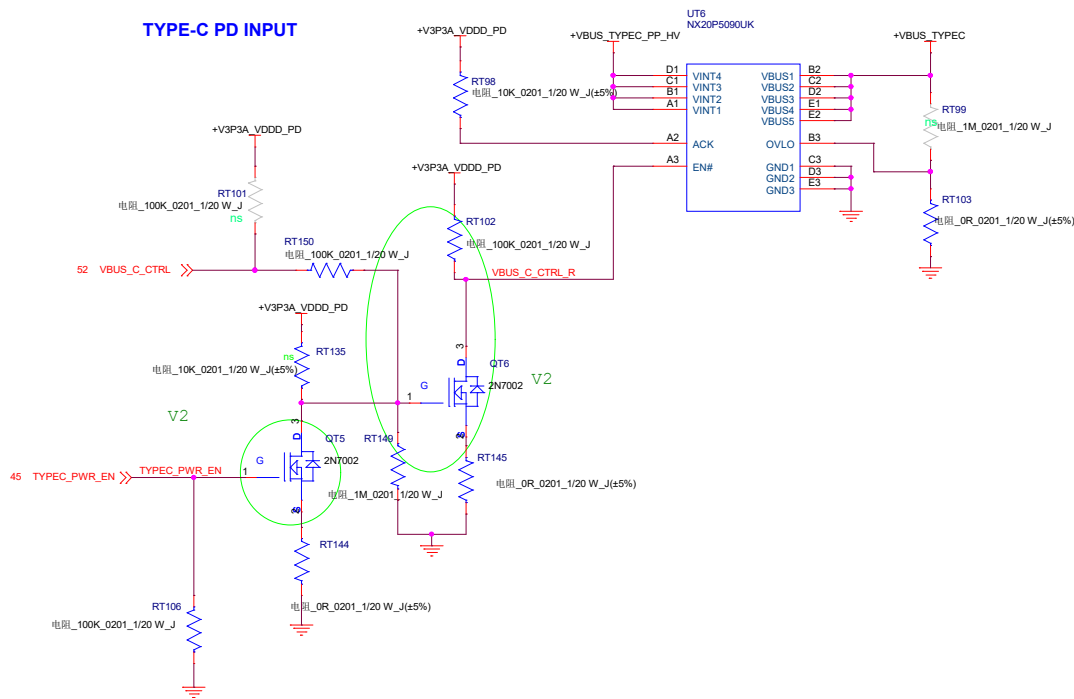




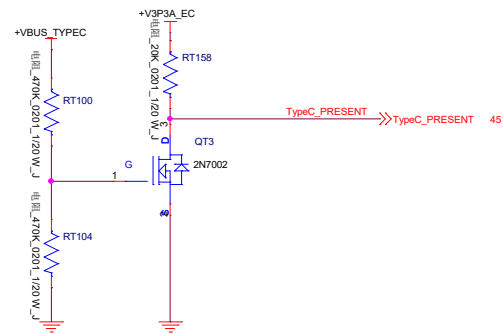


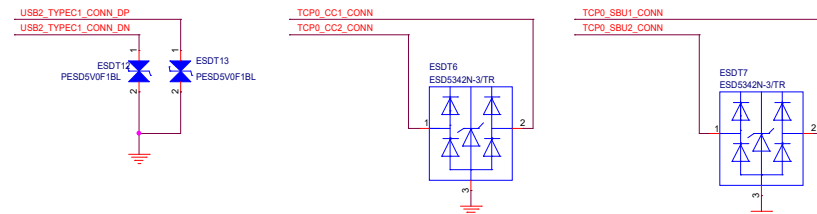
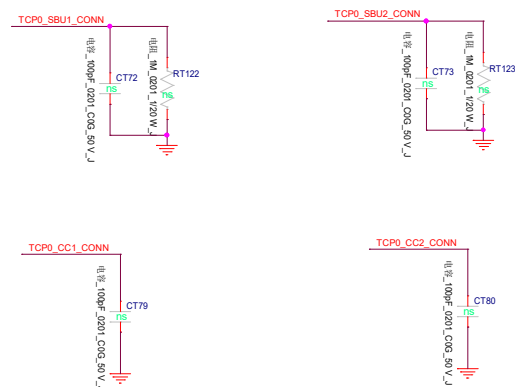
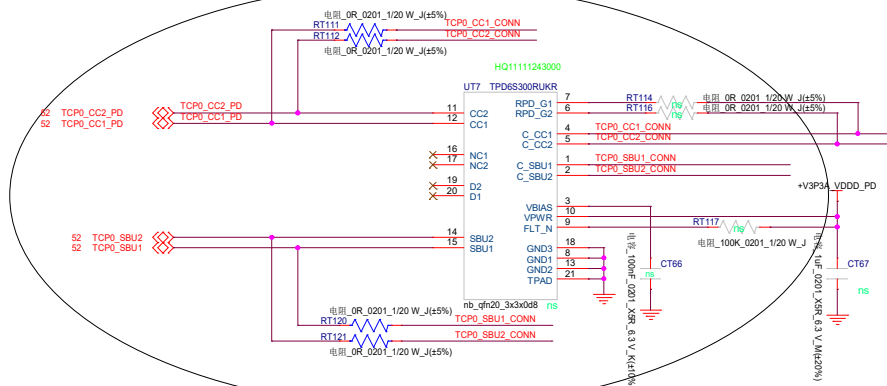
TYPE-C PD OUTPUT

TYPE-C PD INPUT



TYPEC-IN detect

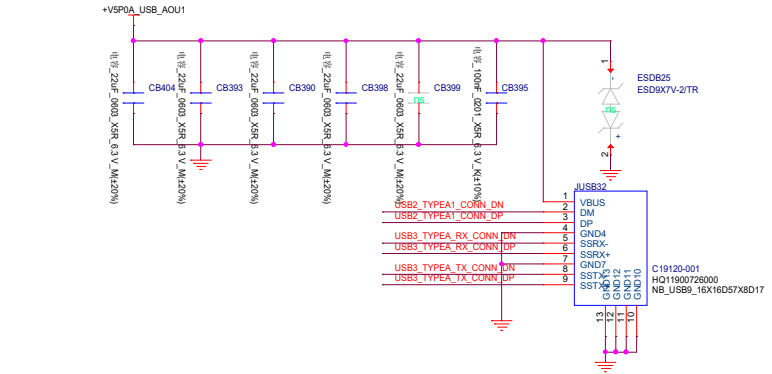




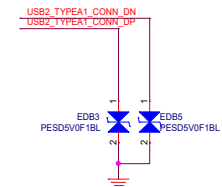
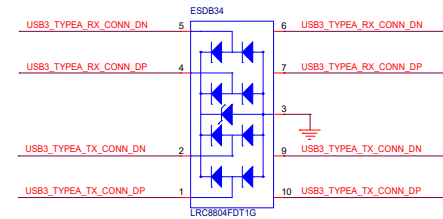
T.ME/SCHEMATICSLAPTOP



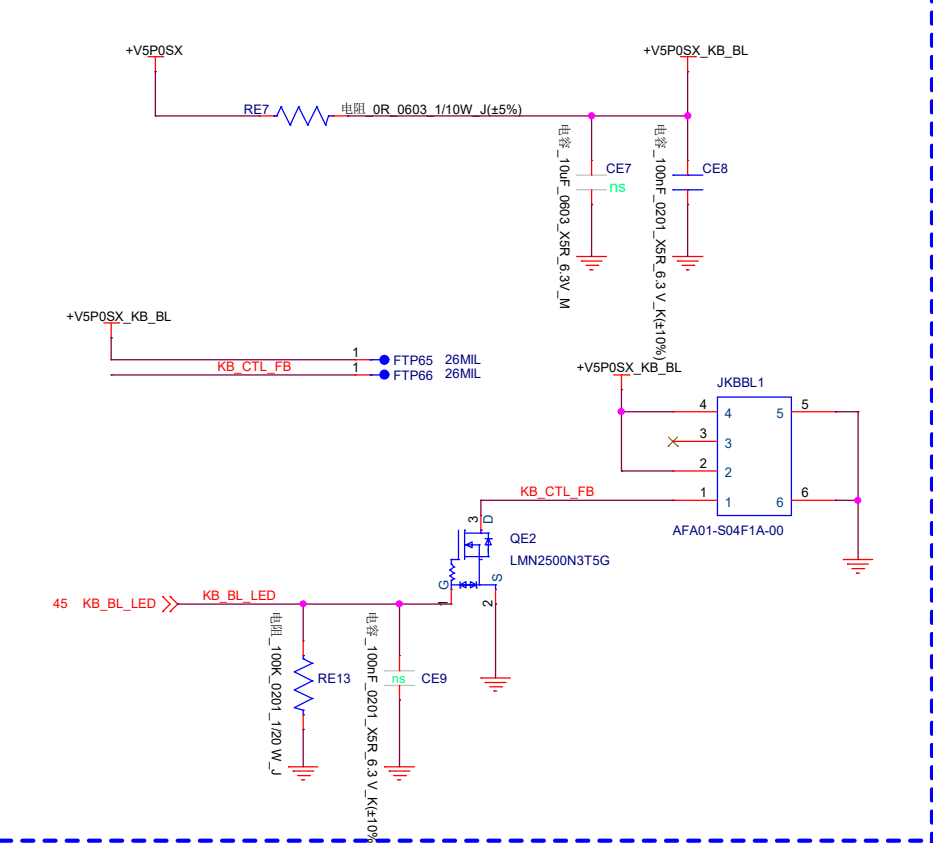
USB3.1 Signal



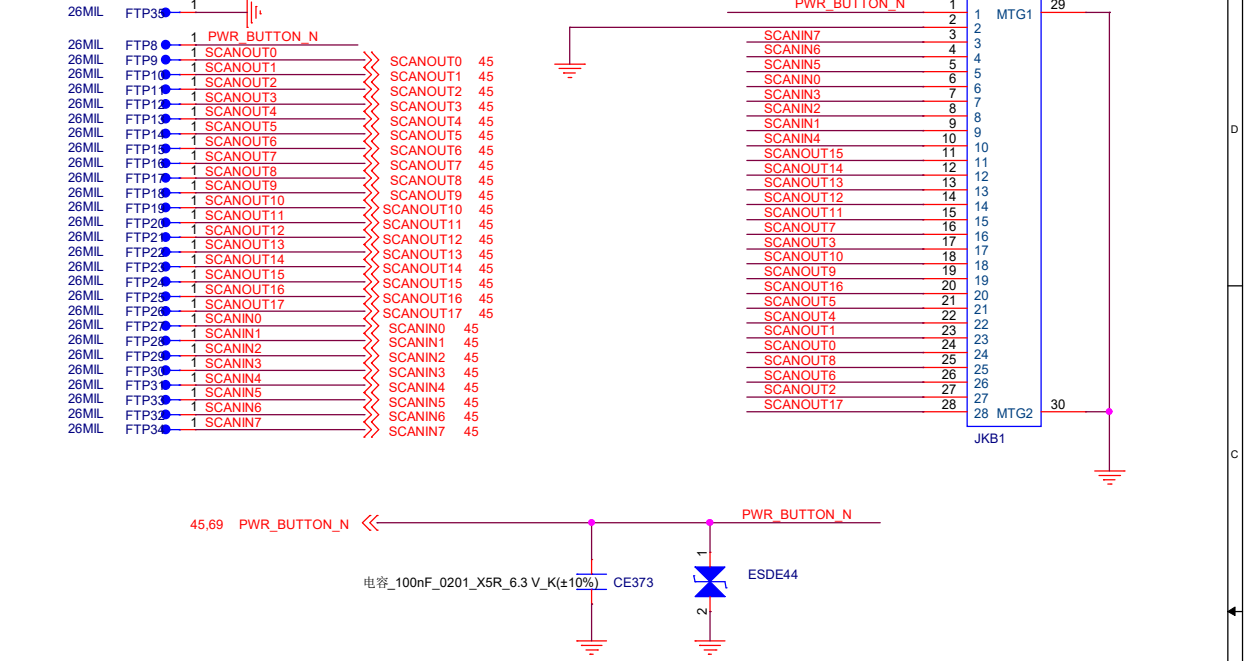
ESDB34



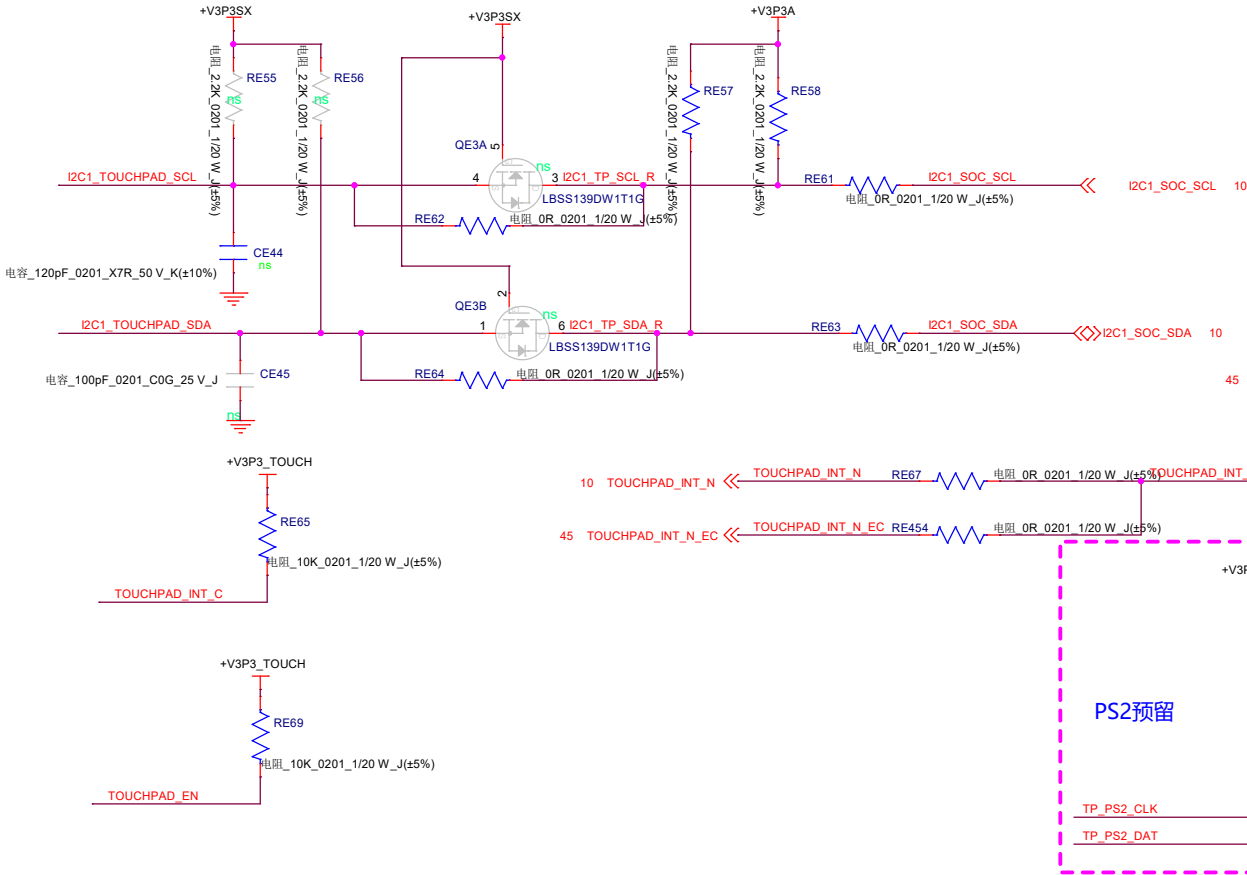
KB Backlight



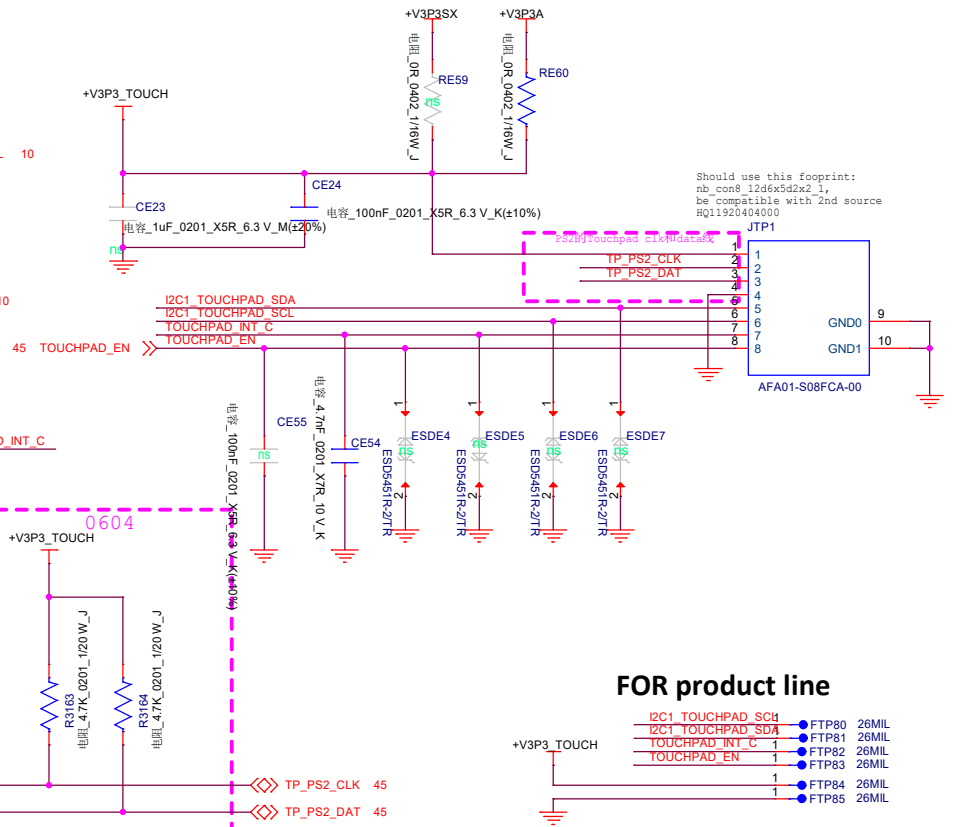
KB CONN



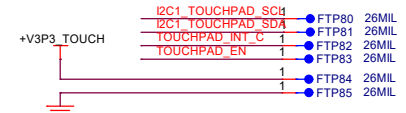
Touch Pad



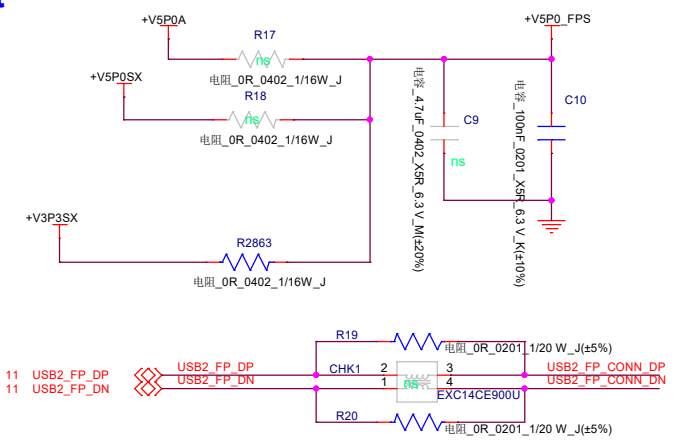
Touch Pad CONN



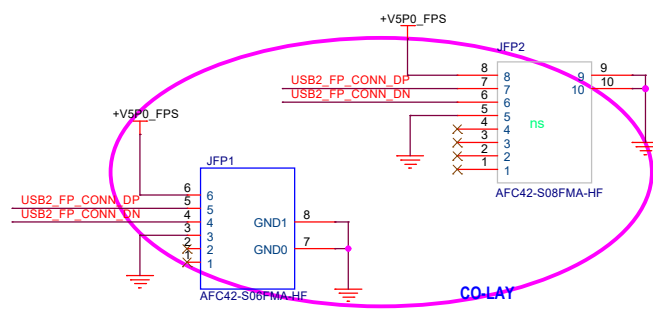
FOR product line



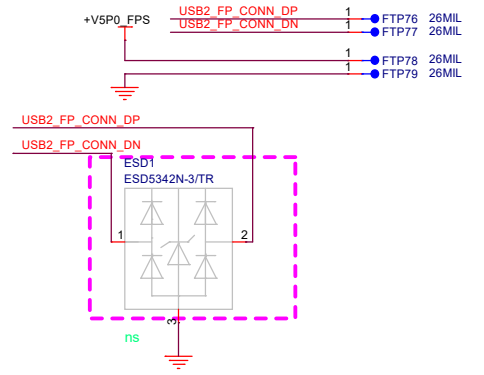
Finger Print



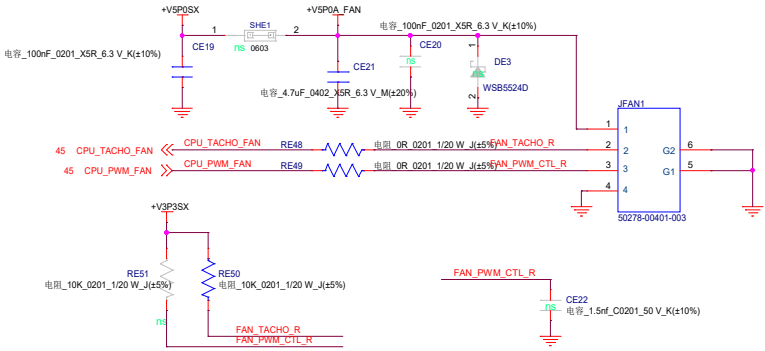
Finger Print CONN



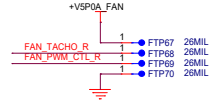
FOR product line



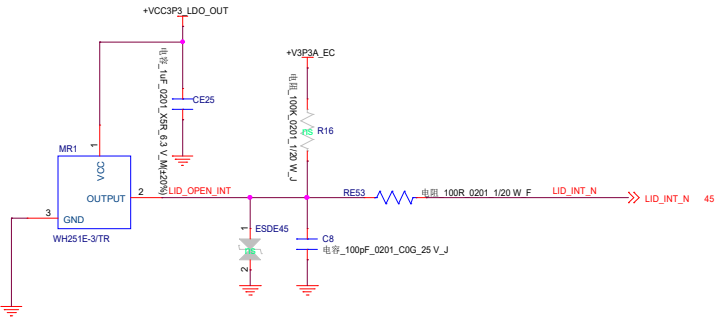
FAN CONN



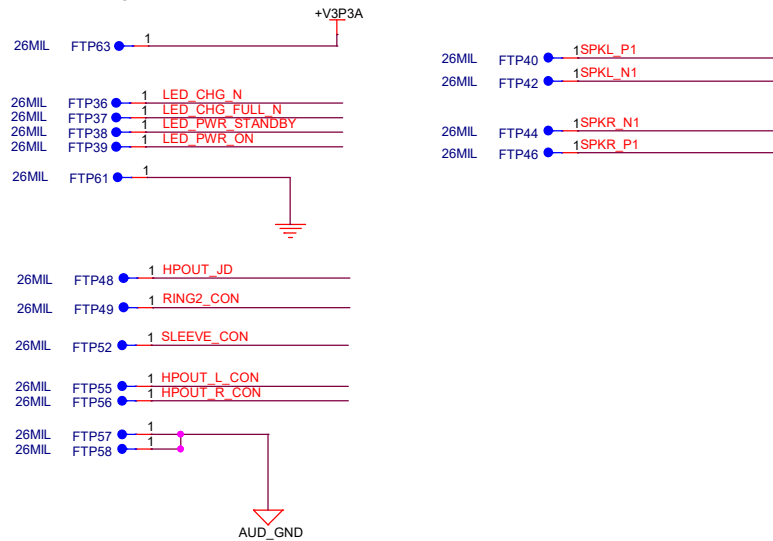
FOR product line



HALL

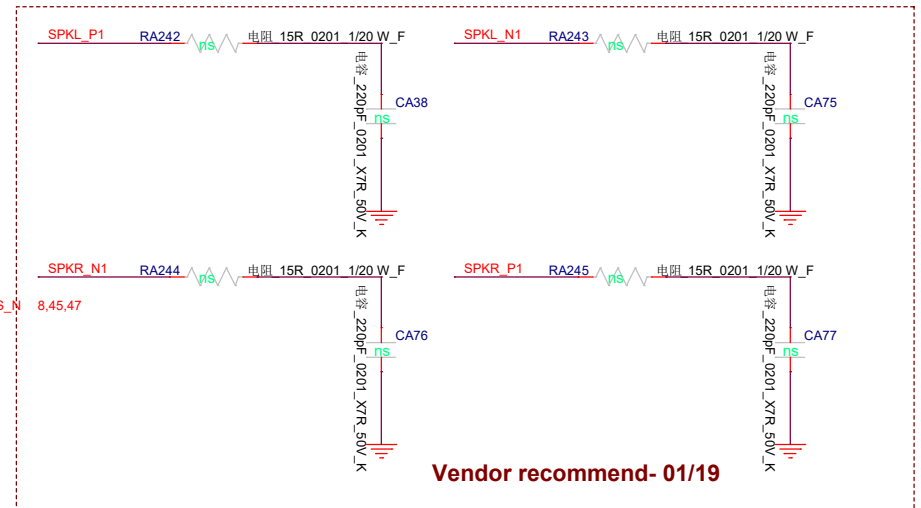
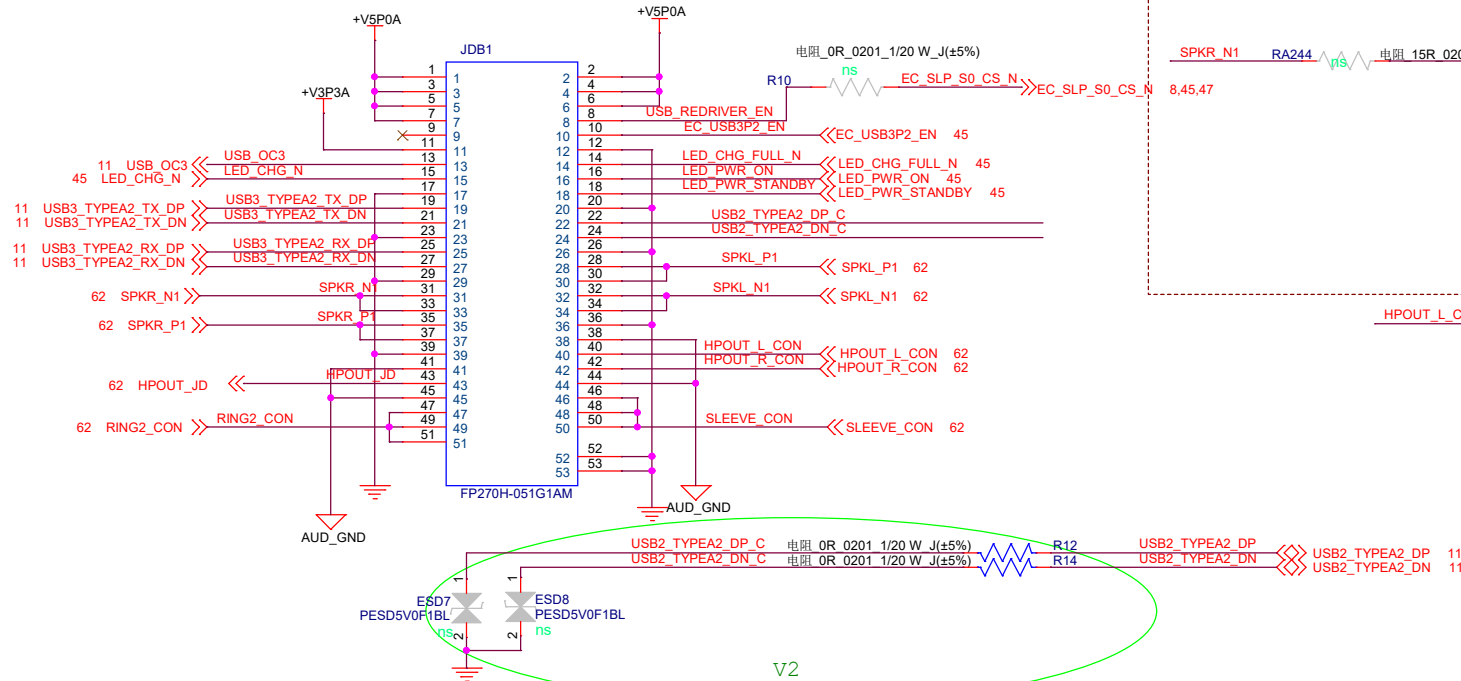
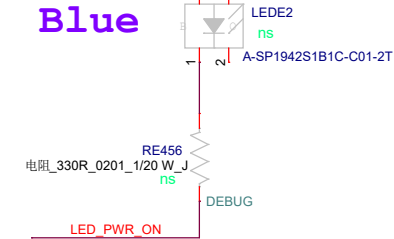



FOR product line



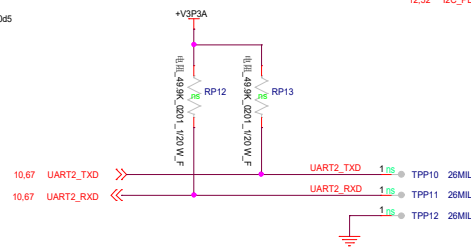
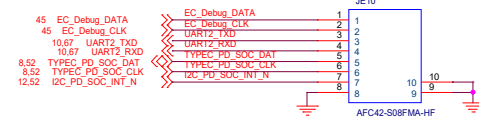
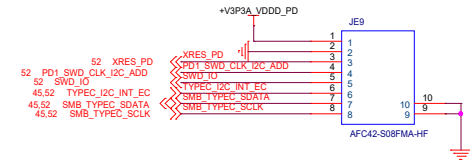
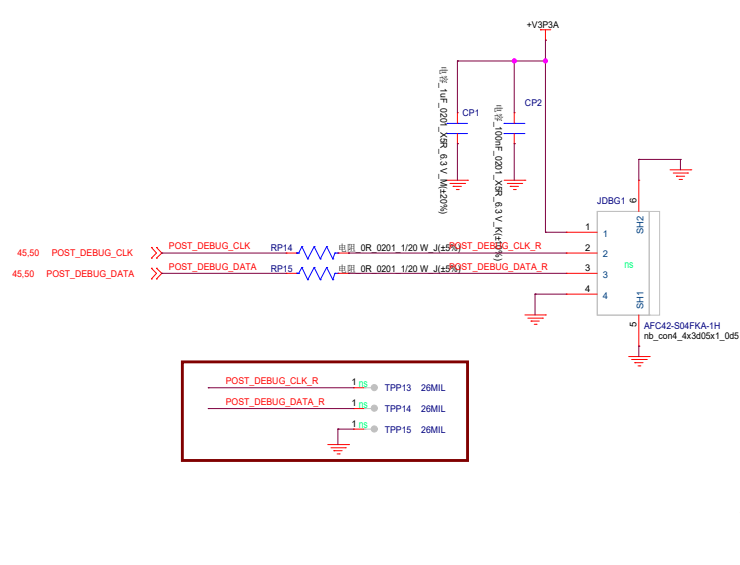
Debug

Blue

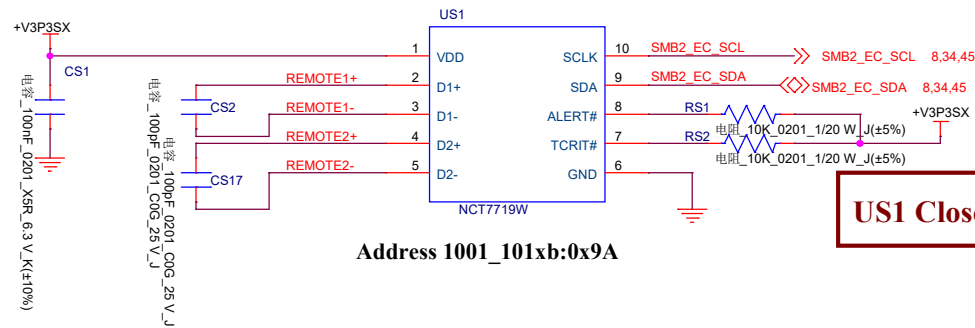


		Huaqin Telecom Technology Com.,Ltd.	
Page name:		DB CONNECTOR	
Size: A4	Project Name:	Swift 3X_TGL-UP3	REV: V4.0
Date:	Thursday, July 09, 2020		Sheet: 66 of 84

CMC

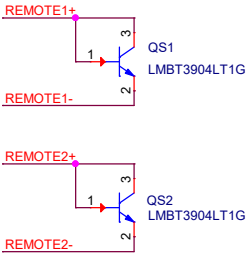


REMOTE1+/-, Trace width/space:10/10 mil,Trace length:<8"
Connect guard traces to GND on either side of the
DXP-DXN traces



Address 1001_101xb:0x9A

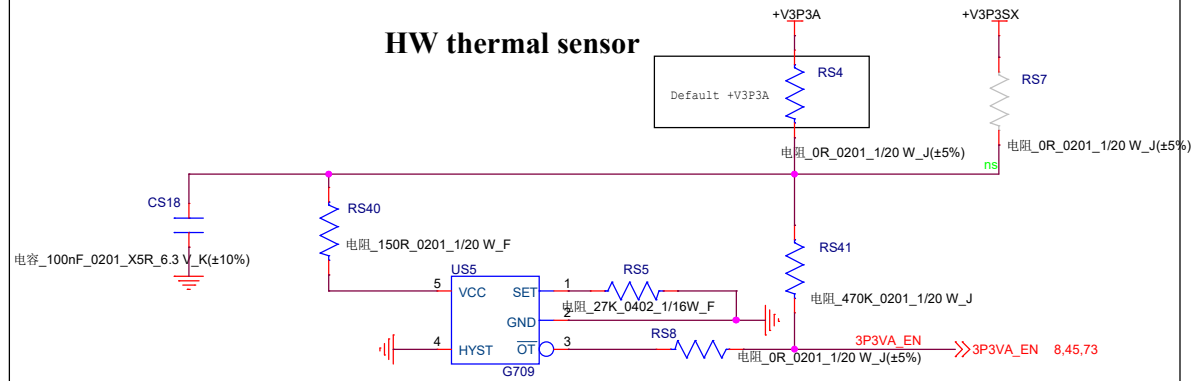
US1 Close to charger



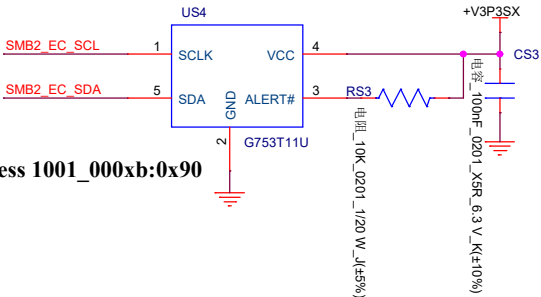
QS1 Close to GPU

QS2 Close to CPU


HW thermal sensor



Address 1001_000xb:0x90



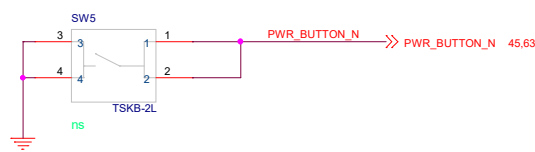
US4 close to SSD

		Huaqin Telecom Technology Com.,Ltd.	
Page name: Thermal sensor			
Size: A4	Project Name: Swift 3X_TGL-UP3	REV: V4.0	
Date: Thursday, July 09, 2020	Sheet: 68	of 84	

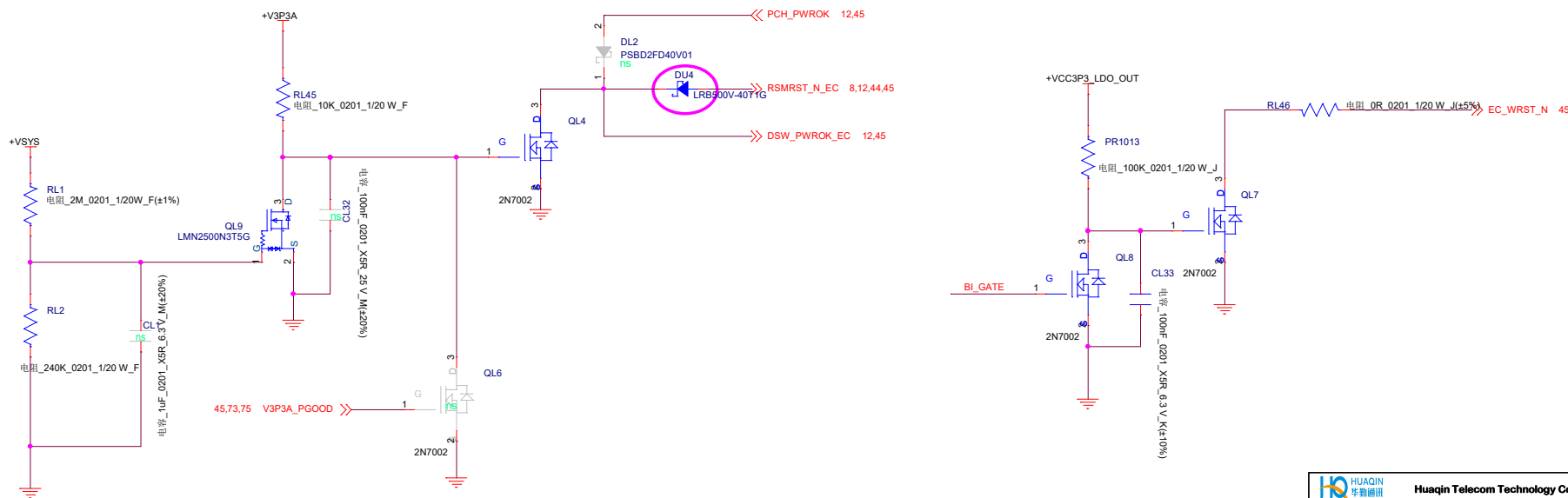
Reset BUTTON



Debug PWR BUTTON

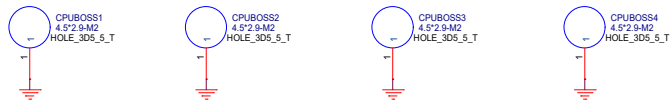


Abnormal PD logic



	WIFI	CPUBOSS1	CPUBOSS2	CPUBOSS3	CPUBOSS4	GPUBOSS1	GPUBOSS2
对应螺丝孔	TH8	TH9	TH10	TH11	TH12	TH13	TH14

CPU螺母元件 *4



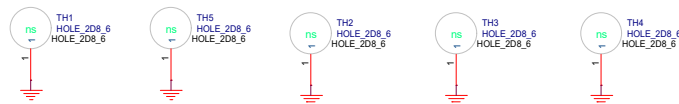
WIFI螺母元件 *1



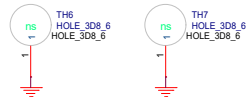
GPU螺母元件 *2



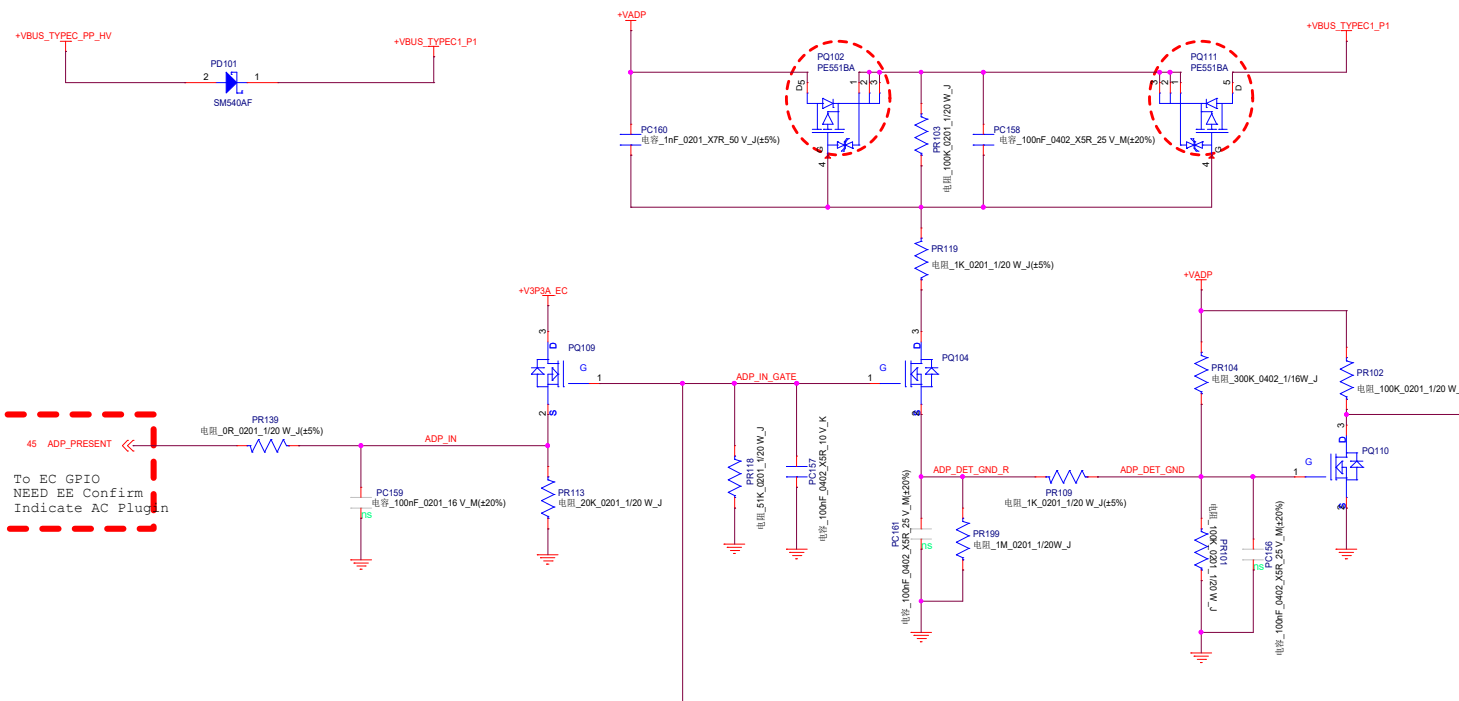
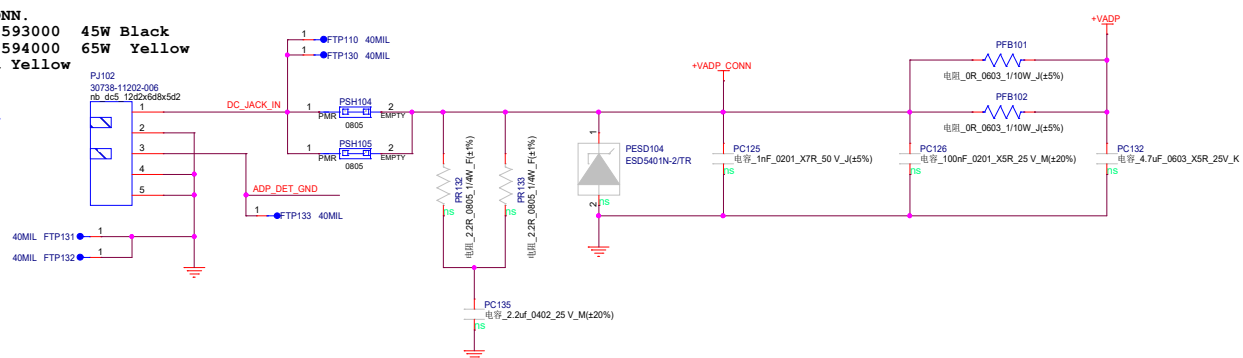
HOLE *5



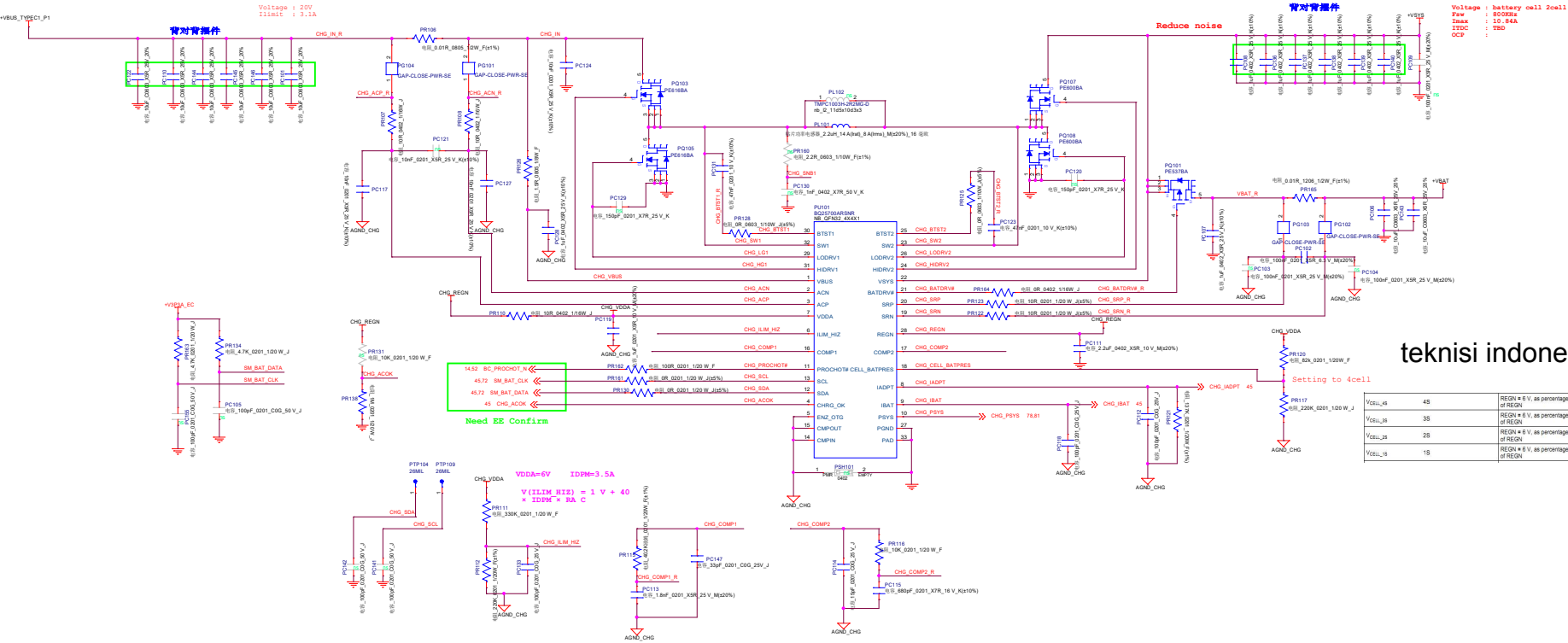
HOLE *2



DC-IN

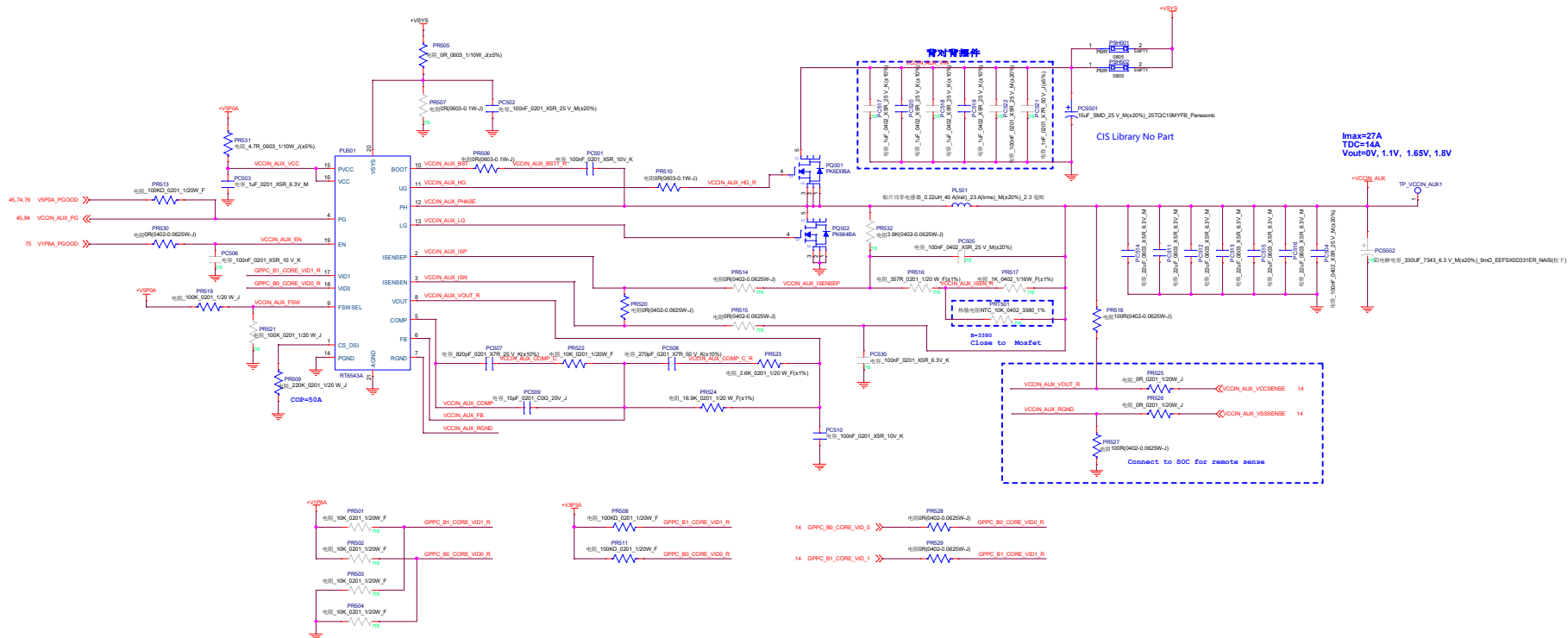


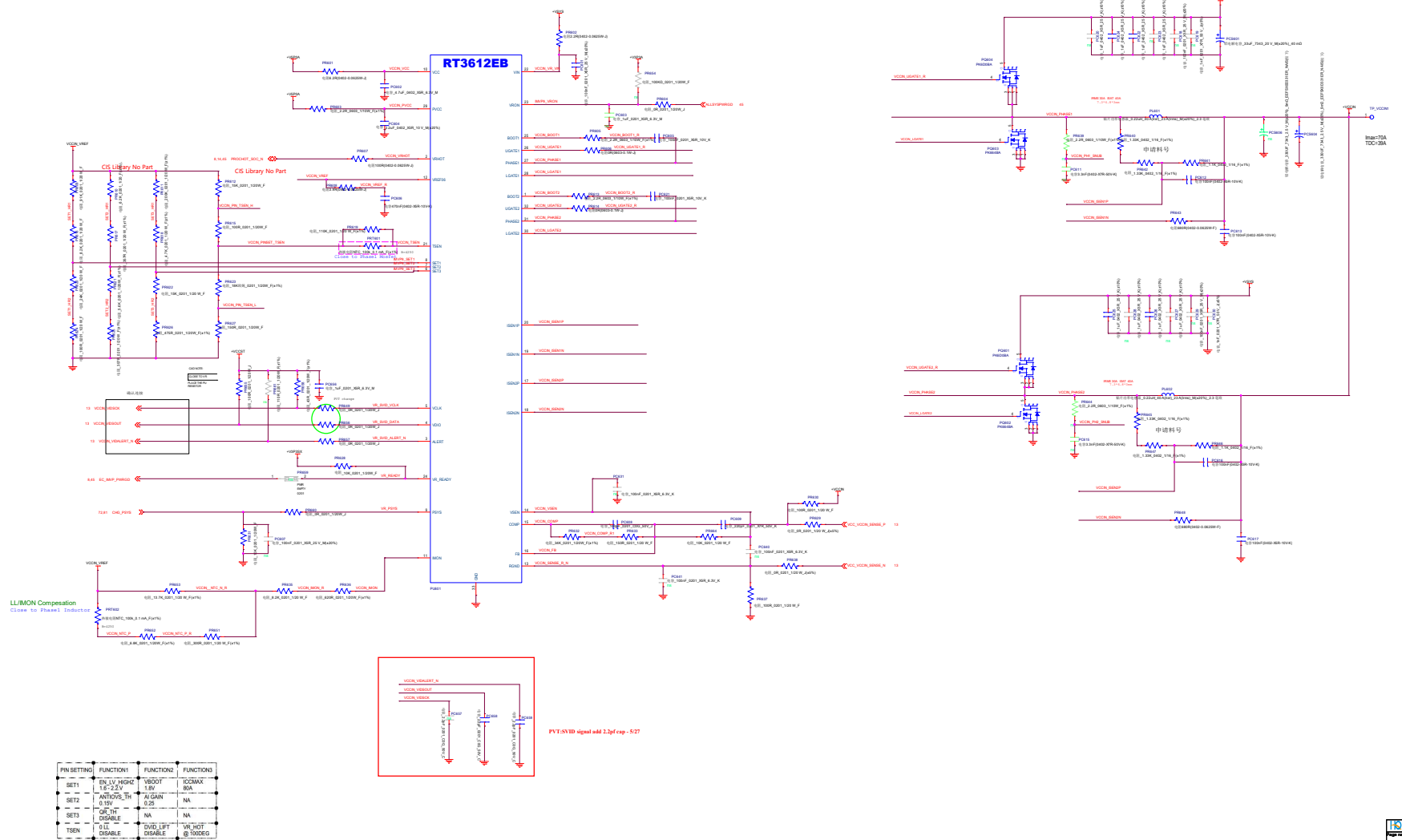
Charger

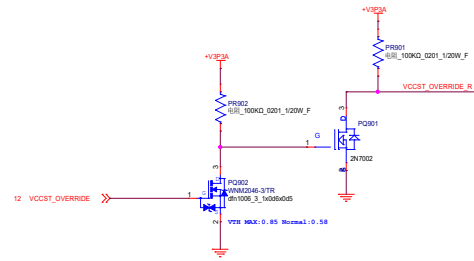
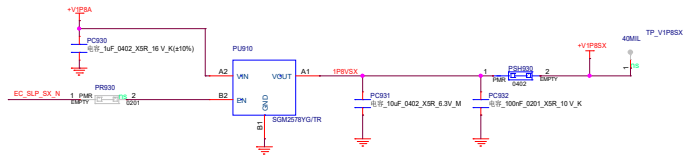


teknisi indonesia

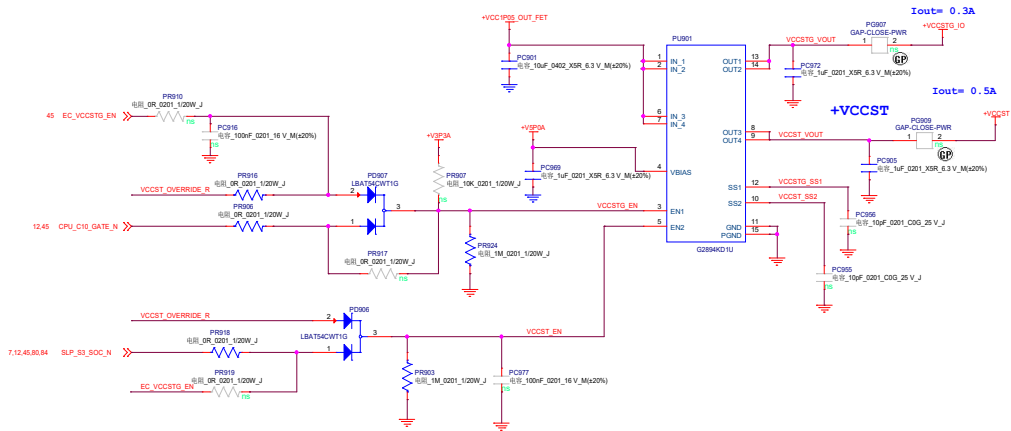
V _{CELL_45}	45	REGN = 6 V, as percentage of REGN	68.4%	75%
V _{CELL_35}	35	REGN = 6 V, as percentage of REGN	51.7%	55%
V _{CELL_25}	25	REGN = 6 V, as percentage of REGN	35%	40%
V _{CELL_15}	15	REGN = 6 V, as percentage of REGN	18.4%	25%



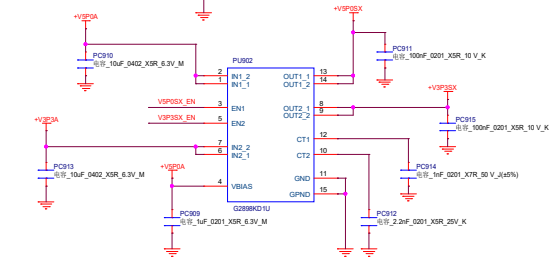


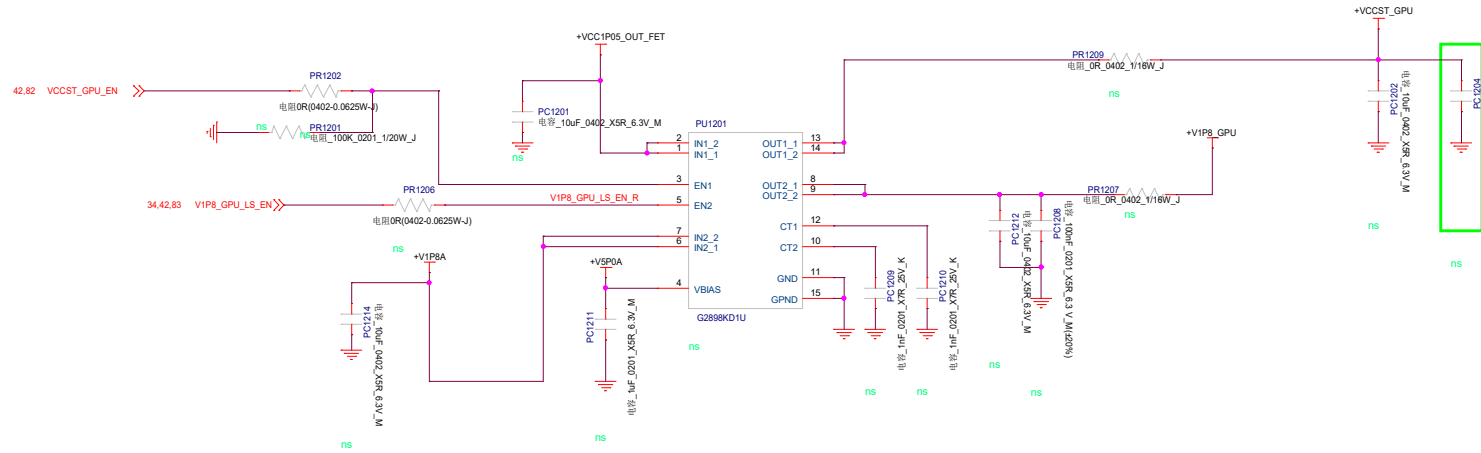
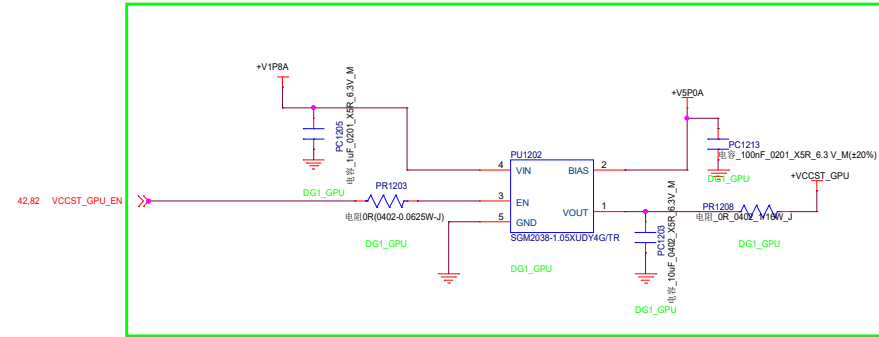


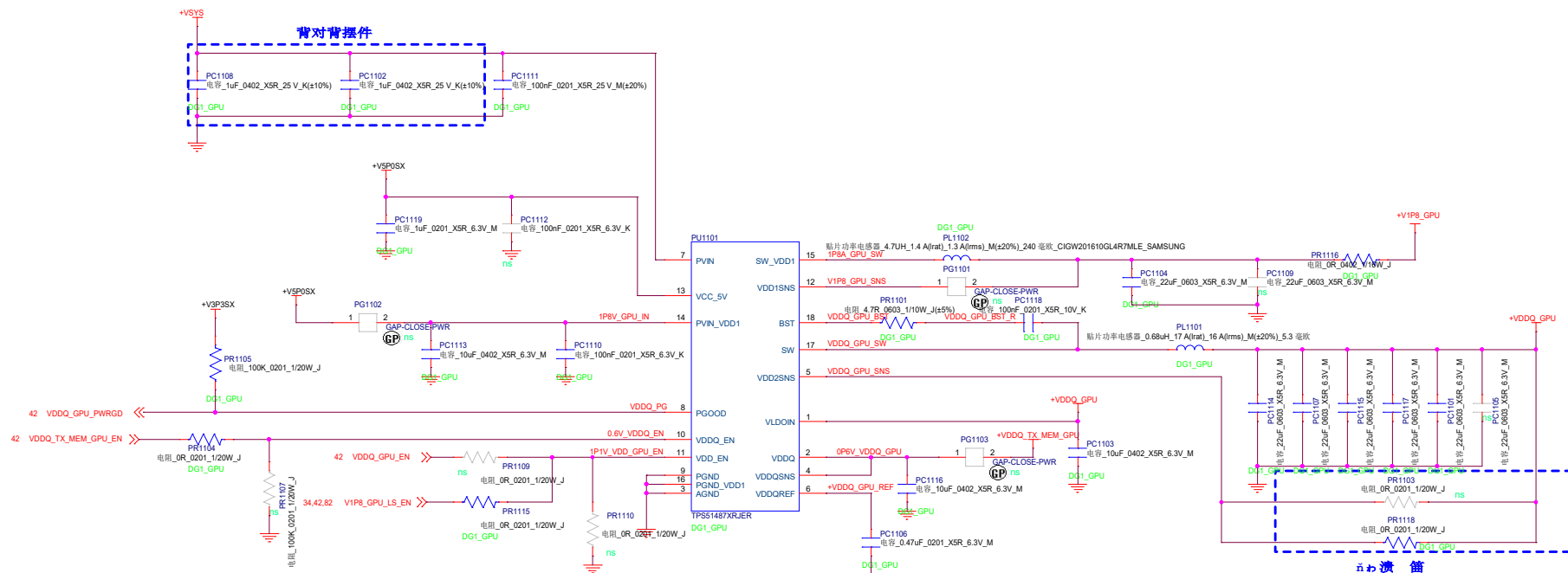
+VCCSTG_IO



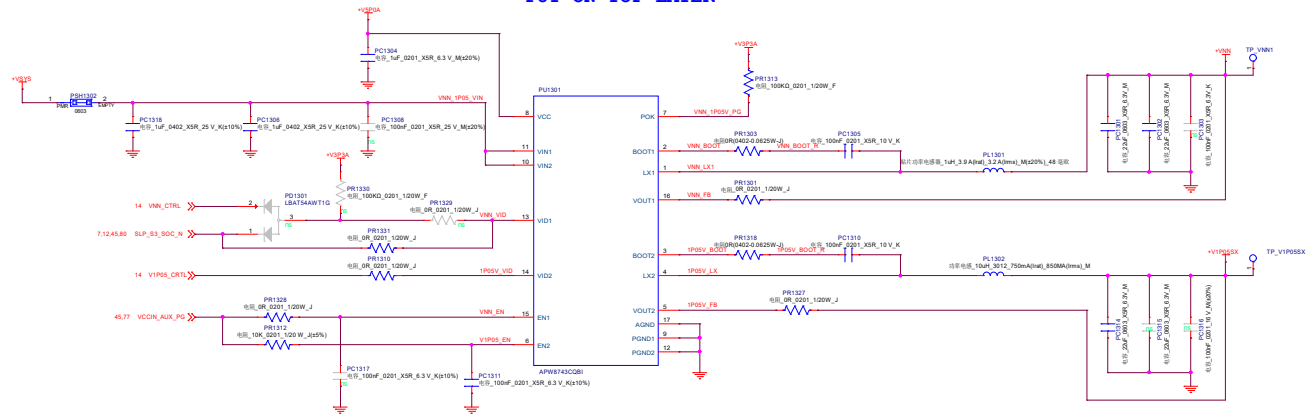
+V3P3SX, +V5P0SX G2898








PUT ON TOP LAYER



20	修改SLP_SUS_N为SLP_SUS_SOC_N	20200120	
21	换SSD和WLAN连接器	20200120	
22	CIS update	20200120	
23	去掉U1及周围几个阻容器件	20200121	
24	USB3和HDMI连接器换了	20200204	
25	2rom的CS0和3.3V电源短路，加一个测试点更正过来	20200204	
26	SLP_WLAN_SOC_N网络加RU435电阻100K下拉	20200211	
27	RO20和RO2之间加网络名SPI_FLASH_CS0	20200211	
28	去掉RO38	20200211	
29	RO27和RO28只连接了1个pin，另一个pin分别连接网络SPI_FLASH_MOSI和SPI_FLASH_MISO	20200211	
30	RF3, RF4, RF5由原来直连CPU，现在改成SPI_FLASH_CLK，SPI_FLASH_MOSI，SPI_FLASH_MISO	20200212	S5项目有 SPI超长问 到J3001的
31	接RO35的网络由SPI_FLASH_CS0_IC改为SPI_FLASH_CS0，增加RO43和RF12	20200212	
32	增加RO38, RO39, RO40, RO41, RO42	20200212	
33	SPI_SOC_CS1网络接到CPU	20200212	
34	RA247电阻NS掉，RU369，RU366和RU367上件	20200214	intel
35	增加RU436和RV278，增加预留电阻RE501	20200214	intel
36	增加RT144, QT6和RT145，且RT144要ns掉，RT101改为上件	20200214	intel
37	增加RT146，ns掉电阻RT56	20200214	intel
38	RT66上件，RT60改为ns	20200214	intel
39	RU41和RU42改为499ohm	20200214	intel
40	增加RT147和RT148	20200214	intel
41	RT59改为ns，RT61改为上件，RT62改为ns	20200214	intel
42	RT78改为上件	20200214	intel
43	增加RV279	20200214	intel
44	删除RE497，ns掉	20200214	intel
45	QV45换了型号，并2和3pin接线互换，且预留RU437	20200214	intel
46	QV39，QV27换了型号	20200214	intel
47	ns掉RV276	20200214	intel

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Page name: Changelist			
Size: A4	Project Name: Swift 3X_TGL-UP3	REV: V4.0	
Date: Thursday, July 09, 2020	Sheet: 85	of 85	